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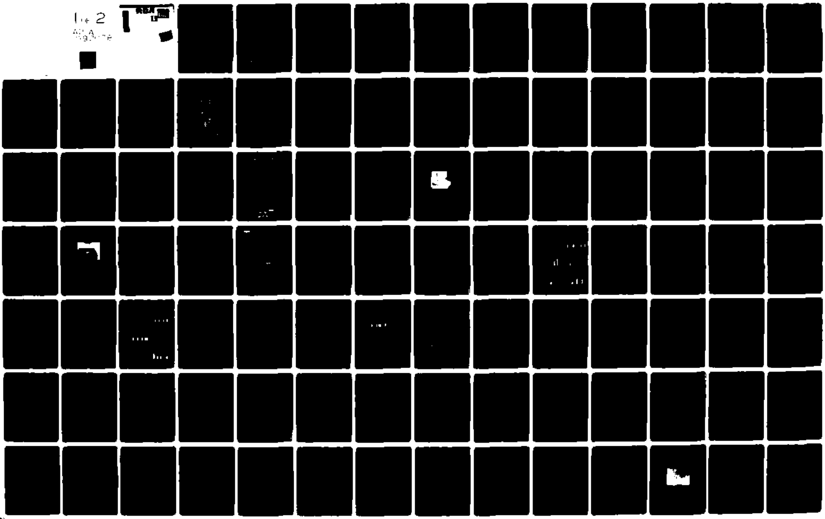

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High Current Rectifier
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High Voltage Rectifier
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RCA has successfully completed the fabrication and testing of fifteen sample devices under this contract. This report thoroughly describes and discusses the assembly and process procedures; test circuits and test results; and configuration management procedure. It also includes numerous detailed drawings and graphs to further illustrate the ingenuity of this Silicon Transcalent Rectifier.

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This report thoroughly describes the test results as well as the basis for selecting the prototype design. It also includes a picture or block diagram of each test circuit utilized. All devices passed all inspections with a yield of 100%.

MANUFACTURING METHODS AND TECHNOLOGY MEASURE
FOR FABRICATION OF SILICON TRANSCALENT RECTIFIER

Final Technical Report

Period Covered: 30 June, 1978 through 31 March, 1980

Purpose of Study: The objective of this Manufacturing and Methods Measure is to establish the technology needed to fabricate Silicon Transcalent Rectifiers.

Contract No. DAAK70-78-C-0120

Prepared by:
B. B. Adams
M. F. DeVito
R. E. Reed

ABSTRACT

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I. Introduction

This report is the Final Technical Report describing the work performed by RCA, Lancaster, PA, during the engineering and confirmatory phases of the contract and covering the period of 30 June, 1978 through 31 March 1980. Work was performed in accordance with the DRME-EA Purchase Description, dated 16 November 1977 (as modified by Amendment No. P00004) to the MERADCOM Semiconductor Device, Silicon Transcalent Rectifier Specification, dated 6 June 1978, as attached to the contract. The scope of the contract covers the manufacturing methods and technology (MM&T) tasks for fabricating a semiconductor device, silicon Transcalent rectifier, RCA type J15401 and the subsequent plans for the pilot production of the device.

This program established the production engineering techniques and plans for a pilot production capability for the J15401 silicon Transcalent rectifier conforming to Figure 1 of this report. Electrical, mechanical, thermal, and environmental inspections are part of this report per DD1423 of this contract.

The pilot run portion of the program was deleted as indicated in the RCA proposal No. DP-8135A for: "Manufacturing Methods and Technologies for Silicon Rectifier", dated 19 November 1979. The subject proposal indicated that the data for the Pilot run report would be an extrapolation from the previously completed Thyristor MM&T Contract No. DAAB07-76-C-8120 as modified by the experience gained in the first two phases of the present rectifier MM&T contract.

The extrapolated data is included in the Preliminary Pilot Run Report (Sequence No. A006) and General Report on Step II (Sequence No. A007), DD1423 issued in June 1980. The two reports were combined into one document.

The Preliminary Pilot Run Report is to verify the contractor's capability to fabricate, at a production rate of ten units per eight hour day, Transcalent Silicon Rectifier type J15401. The report includes flow charts and covers the preliminary plans by the contractor to establish the process and fabrication controls as well as the testing required to produce pilot run units at the specified rates.

The step II portion contains a production graph showing the time to produce the first Silicon Rectifier Device and to reach production rate goals. Background information is presented which indicates the contractor's production plans to reach a specified production rate goal.

II. Device

A. Description of the Structure

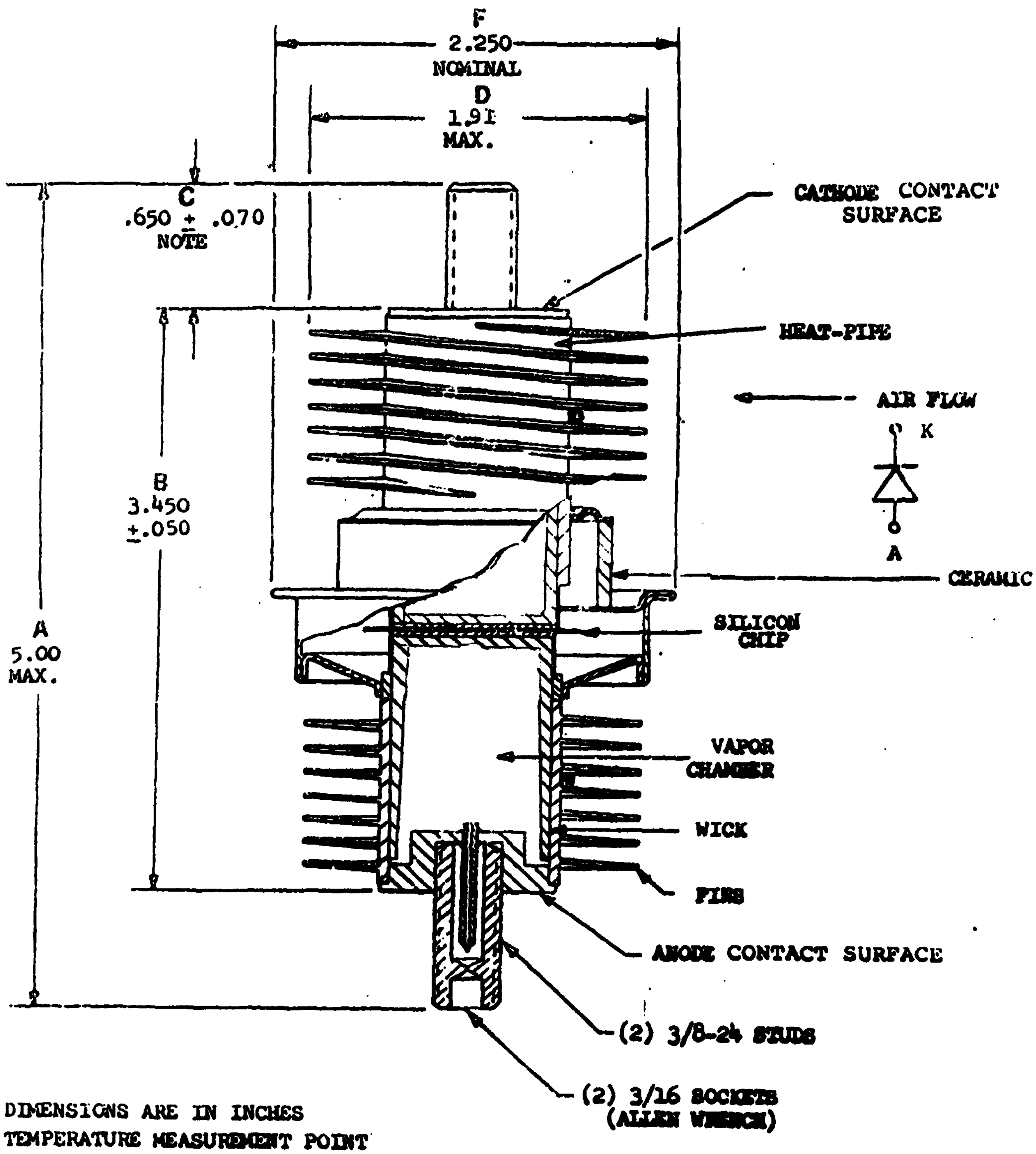
The Transcalent rectifier type J15401 is designed to make maximum use of the integral heat-pipe thermal package developed previously for the Transcalent rectifier.[1] A cross-section of the device is shown in Figure 1 with a heat-pipe attached to each side of the silicon chip. In operation, current is conducted to and from the silicon chip by the low inductance, high conductivity copper heat-pipes.[a] The studs at the ends of the heat-pipes are for fastening the high current leads to the device. The gate and auxiliary cathode leads are for attachment of the control signal to the rectifier.

A ceramic insulator and metal envelope is constructed between the two heat-pipes. This envelope is the main structural member joining the two heat-pipes and prevents stress being transmitted to the weaker silicon chip. The envelope also contains an inert dry nitrogen atmosphere around the contoured edge of the silicon chip across which the high blocking voltages of the Rectifier are developed.

Heat which is generated in the silicon chip during operation is conducted into the heat-pipes through the molybdenum disc closing the end of the heat-pipe adjacent to the silicon. The thickness of the molybdenum disc is optimized to have a minimum temperature rise in the silicon wafer during a single cycle of surge current by balancing the

[1] Kessler, S. W., "Development of a 250 Ampere Transcalent Rectifier", Final Technical Report, June 1970, Contract DAAK02-69-C-0609.

[a] U.S. Patent 3,605,074, "Electrical Connector Assembly Having Cooling Capability", Freggens, R. A. and Harbaugh, W. E.



DIMENSIONS ARE IN INCHES
* TEMPERATURE MEASUREMENT POINT
NOTE - THREADS - 0.550" MIN.

Figure 1 Transcalent Rectifier Type J15401 Cross Section Drawing absorption and transfer of the heat.[b]

Next, the heat is transferred into the porous copper wick adjacent to the molybdenum disc. The pores of the wick are filled with water which, when evaporated, transfers heat to all parts of the heat-pipe by its latent heat of vaporization. Since the heat-pipe is an evacuated vessel, evaporation occurs at all temperatures, (including below freezing by sublimation) and the vapor pressure curves of water. When the vapor condenses at the coolest point in the heat-pipe, the vapor gives up its latent heat of vaporization. The condensation heat is conducted though the wall of the heat-pipe to the fins and dissipated to the air by the cooling fins. Since the vapor condenses at the coolest point, the heat-pipe is essentially isothermal with equal amounts of heat being dissipated with equal efficiency by all of the fins. The condensate is returned to the evaporator by the capillary forces of the pores of the wick.

This double-sided heat-pipe cooled rectifier is inherently rugged and has unique advantages. Applications experience with Transcalent devices had demonstrated their superiority over "hockey-puck" or "stud-mounted" devices, namely:

1. There are no mechanical clamps fastening the device to the heat sink. Industrial experience indicates that the clamping force relaxes through creep of copper and aluminum during the life of the "hockey-puck" rectifier. Inadequate cooling and lossy electrical contacts may result.

2. Heat is extracted from both sides of the silicon with a minimum of material adjacent to the silicon. This arrangement produces a low-temperature gradient between the junction (which is limited in an SCR by the silicon characteristics to a maximum temperature of 125^{o}C) and the ultimate heat sink.

[b] Kessler, S. W., U. S. Patent 3,984,861, "Transcalent Semiconductor Device, etc."

3. The thickness and the thermal properties of materials adjacent to the silicon are optimized to absorb the transient surges of power that must be dissipated from the silicon if blocking and control characteristics are to be maintained.

4. In operation the heat-pipes are very tolerant to changes in power level because of their ability to respond quickly by evaporating an additional amount of working fluid. They exhibit a decreasing thermal resistance as the power level increases.

5. The assembly has a high resistance to fatigue failure because the materials adjacent to the silicon and bonded to it either match the thermal expansion of the silicon or are designed to yield elastically. By comparison, the rubbing surfaces of a clamped device are subject to fretting and scoring.[3,4] As fretting debris accumulates between the clamped surfaces, the contact resistance between adjacent materials increases and alters their electrical and thermal impedances.

6. Operation at higher abient temperature is possible without current derating.

7. Transcalent devices are of smaller size and lighter weight because of the greatly reduced temperature gradient between the junction and the fins. Also, all of the fins are equally effective in dissipating heat because the heat-pipe is isothermal along its entire length.

[3]Comyn, R. H. and Fulani, C. W., "Fretting Corrosion", a literature survey, TR1169, Harry Diamond Labs, Army Material Command Washington, DC, 30 December, 1963.

[4]Comstock, W. R. and Locher, R. E., "High Current Diode and SCR Reliability Considerations", IEEE Power Electronics Specialist Conf. 1975, pp 224-233.

III. Process and Fabrication Improvement

All sample rectifier devices were fabricated utilizing, as much as possible, the recommendations given in RCA proposal DP-8135, and the description given in this report.

A. Engineering Phase

Five engineering samples plus three special rectifiers were fabricated during this phase of the contract.

1. Silicon Wafer Process Improvement

Investigations were completed in three areas of silicon wafer process improvement.

a. Initial Cleaning Investigation

One half of a lot of rectifier wafers, #ER-1, was processed eliminating the initial scrubbing and ultra-sonic cleaning steps. The other half of the lot was prepared following the standard procedures. All of the scrubbed wafers had blocking voltages greater than 1000 V and average leakage currents of 40 μa.

Only five out of nine of the unscrubbed wafers had similar characteristics. The four unacceptable wafers were soft, having leakage currents greater than 1 mA in the voltage range of 1/2 V to 140 V. Therefore, elimination of scrubbing is not advisable.

b. Dopant Deposition

Lot #ER-2 was ion implanted with a boron $N_{dose} = 6 \times 10^{15}$ at 200 Kev on one side and a phosphorus $N_{dose} = 6.5 \times 10^{15}$ at 180 Kev on the other side. One of these wafers and a standard doping process wafer were profiled by successively etching away the silicon down to the junction and checking the resistivity at each step. The profiles are shown in Figures 2, 3, 4, and 5.

Fig. 2 - Ion Implant
Boron
$N_{Dose} = 6 \times 10^{15}$ at 200 Kev.

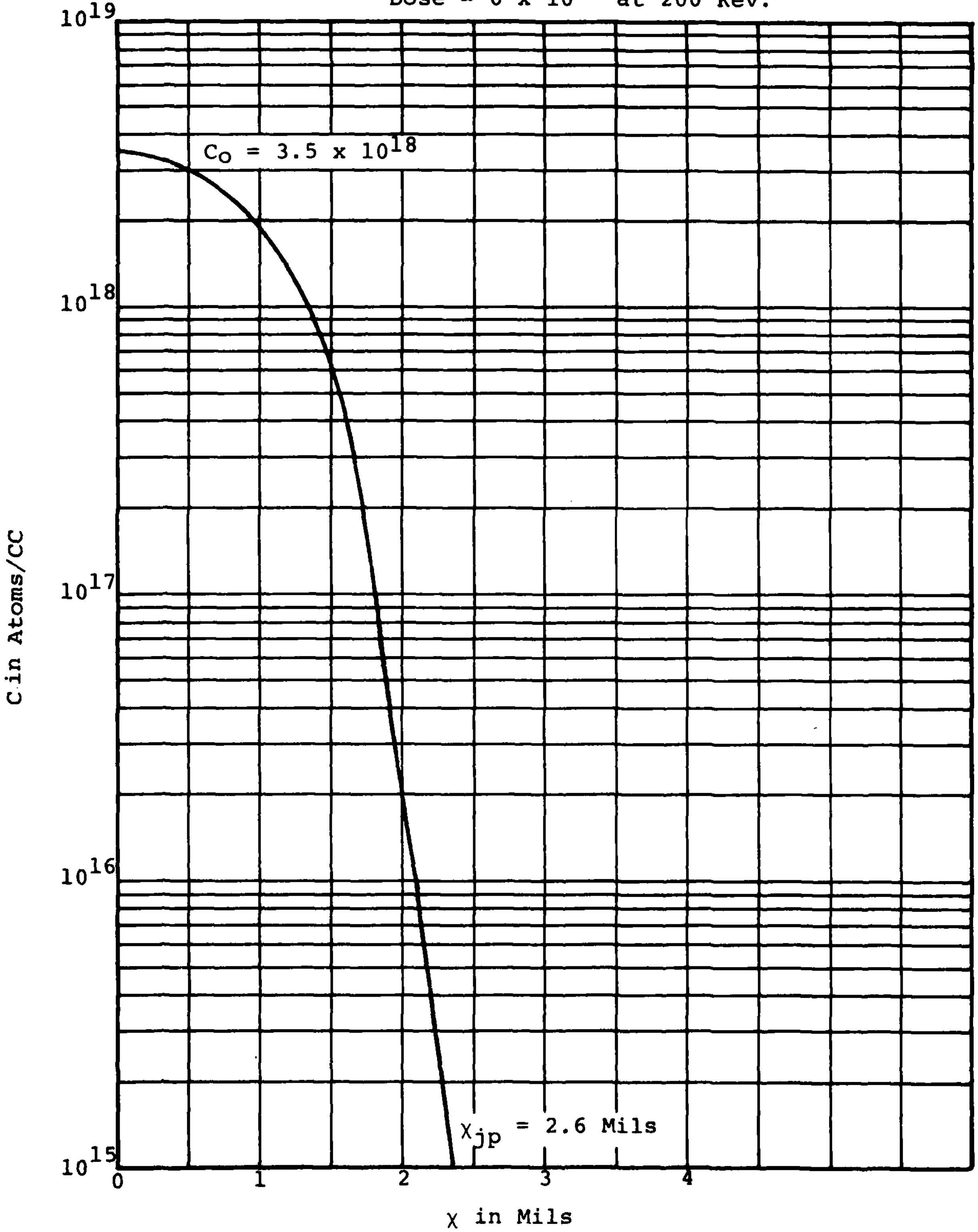


Fig. 3 Ion Implant

Phosphorus
$N_{Dose} = 6.5 \times 10^{15}$ at 180 Kev.

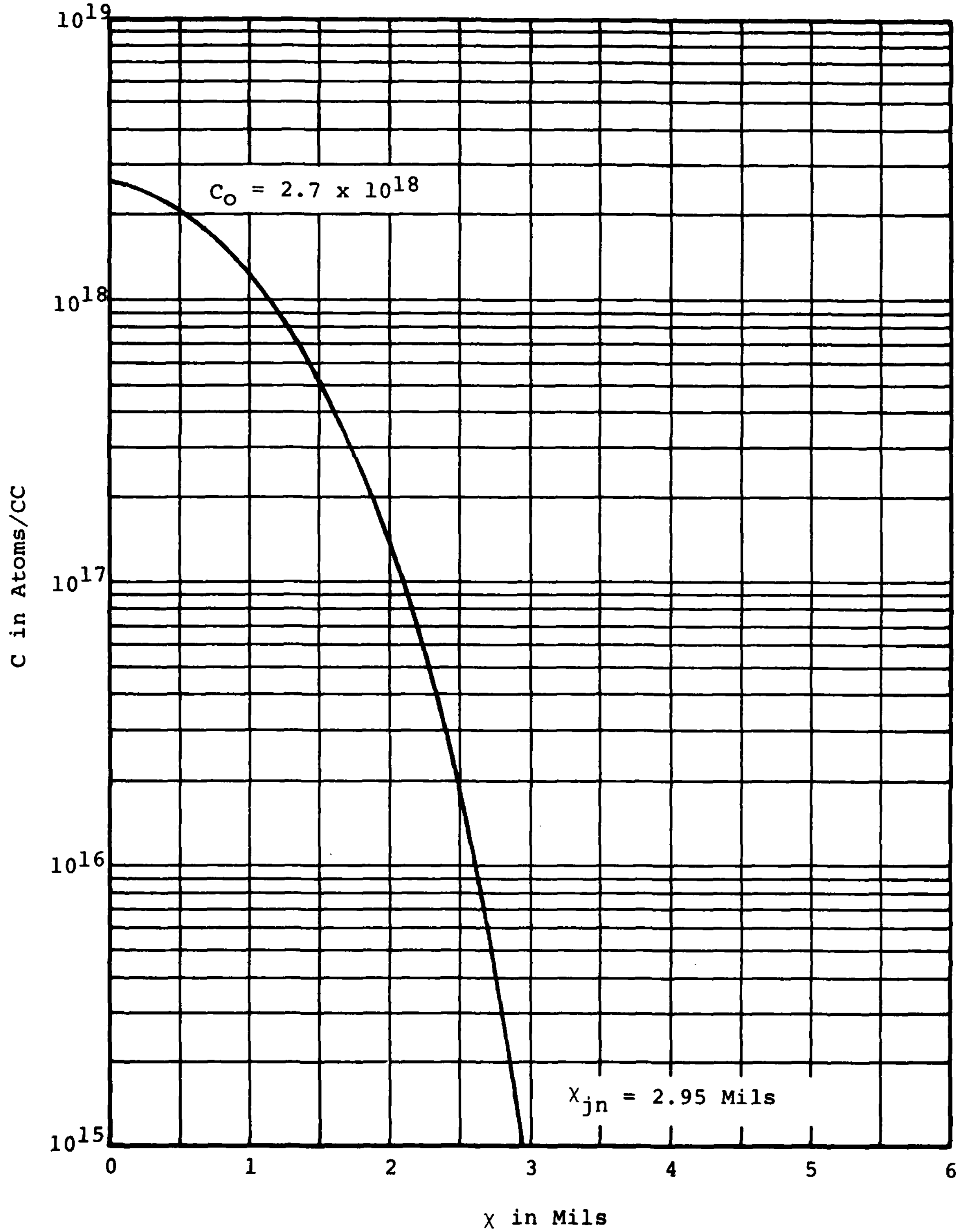


Fig. 4 Standard Doping Boron

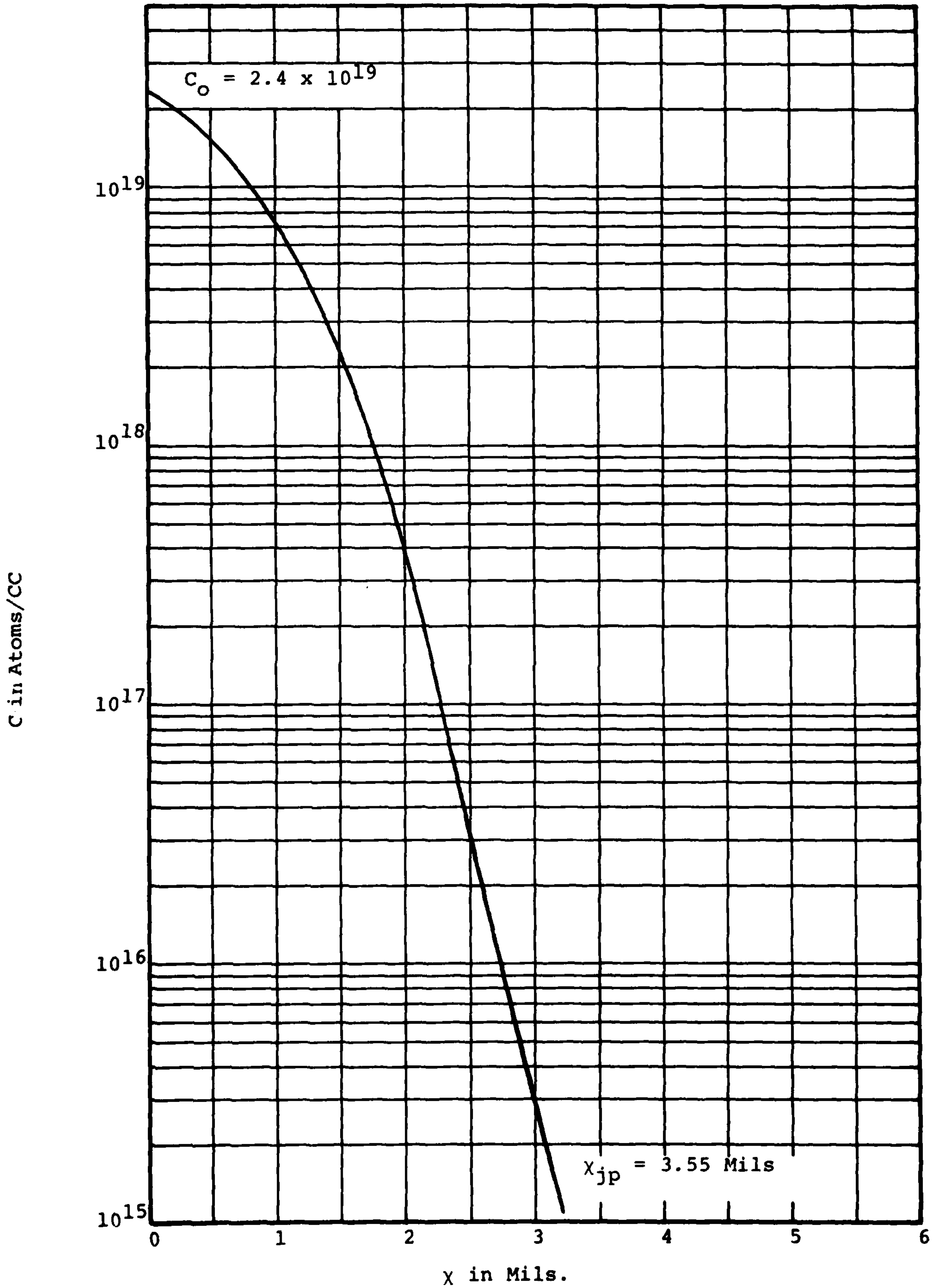
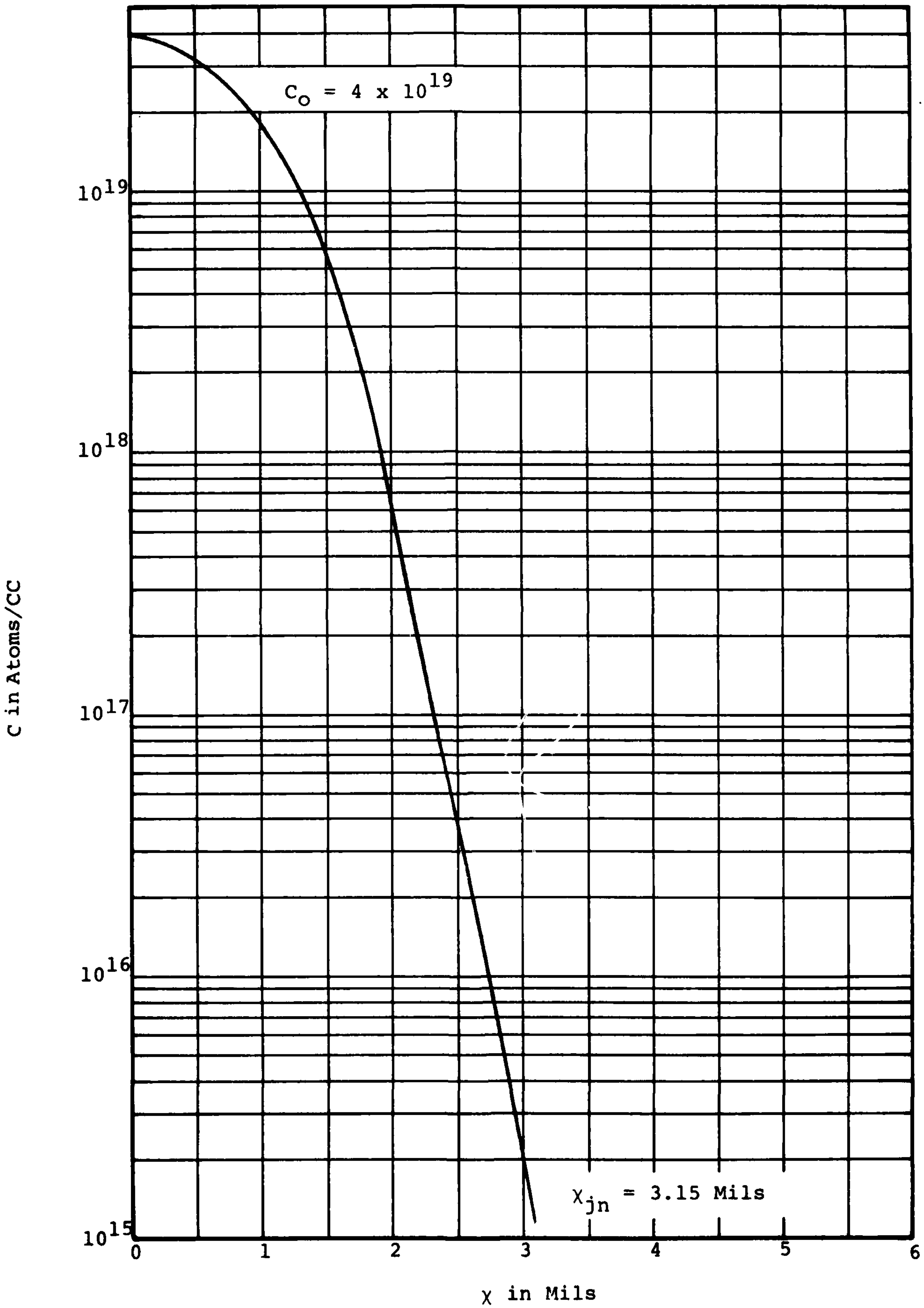


Fig. 5 Standard Doping
Phosphorus



There was no detectable difference in electrical performance of the ion implanted vs. the standard process rectifiers. The ion implantation eliminated five of the nine process steps and substituted the two implants. However, a hot source implanter would be required to implant economically, since the time for implanting the boron was 20 min./wafer using the implanter available.

The contractor will not be buying a hot source implanter, however, the investigation of the constructed units with ion implanted wafers was continued during the confirmatory phase of the contract.

c. Starting Silicon Material

Three lots of rectifiers were processed using wafers that were merely sawed and etched, with no lapping or polishing. Lot #ER-4 used 6.5 mil wafers with standard doping procedures and reduced diffusion time.

Lot #ER-5 used 6.5 mil wafers with ion implantation and reduced diffusion time.

Lot #ER-6 used 10.5 mil (standard thicknesses) with standard doping procedures.

2. Silicon Wafer Metallizing, Contouring and Electrical Testing

The diffused silicon wafer (one chip per wafer) was delivered to the metallizing operation following the polysilicon densification. The purpose of the following sequences was to prepare the wafer for bonding to the heat-pipes as well as to increase the high voltage blocking capabilities of the exposed edge of the chip.

The materials and processes developed for this sequence of operations on the silicon are listed in the following paragraphs. Refinements incorporated during the engineering phase of the MM&T program are also discussed. Refer to the Flow Diagram of Figure 6.

FLOW DIAGRAM FOR THE J15401 RECTIFIER WAFER METALLIZING, CONTOURING & TESTING

Diffused silicon wafer

Clean and evaporate palladium onto both sides

Chemical vapor deposit tungsten onto both sides

Nickel strike and nickel plate wafer

Contour edge of silicon to produce chip

Solder dip chip

Etch contoured edge of chip

Electrical (demountable) test of chip

Deliver to Rectifier Assembly Operation

Figure 6

3. Palladium Evaporation

The wafers were cleaned and a thin layer of palladium was evaporated in a vacuum environment onto both sides of the wafer. Palladium forms a low resistance ohmic contact to the silicon and a strongly adherent palladium silicide when it is diffused into the silicon during the following operation.

4. CVD Tungsten Metallizing

The next layer to be deposited onto the entire wafer was a thin layer of chemically vapor deposited tungsten. Tungsten strengthens the silicon wafer and acts as a base for the subsequent deposition of the solder alloy materials. Tungsten's thermal conductivity is excellent and its thermal expansion more nearly matches that of the silicon than any other structural material.

The tungsten is deposited by reducing gaseous tungsten hexafluoride with hydrogen gas at high temperature in a partial vacuum pressure. The deposition time is several minutes with the pressure varied cyclically to help assure a uniform deposition thickness.

5. Nickel Electroplating

The wafers were electro-nickel struck and plated on both sides to an adequate thickness for soldering. Standard nickel strike and nickel plating chemical solutions were used and a holding fixture was employed to make simultaneous contact to a multiple number of wafers. The number of silicon wafers plated with nickel can be easily increased by the paralleling of a greater number of wafers in this plating circuit.

The metallizing of the diffused silicon wafers consists of three layers (palladium, tungsten and nickel) of metals for a grading of the physical properties between the silicon and the heat-pipes. Refer to Figure 7 for a cross-section drawing of the metallized wafer.

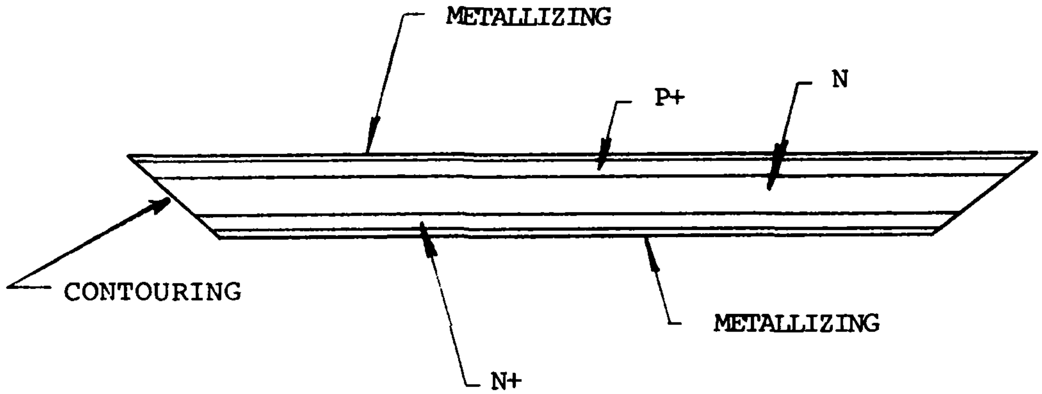


Figure 7 Cross-Section of the Metallized and Contoured Rectifier Wafer

6. Contouring to Produce the Chip

The silicon chip was cut from the metallized wafer by using a finely divided aluminum oxide abrasive propelled by high pressure air. The abrasive was directed against the wafer which was waxed to a holding mandrel while being rotated at high velocity. The precision nozzle which directs the abrasive was positioned so that both the diameter of the chip and the positive contour angle were cut as the abrasive bore through the thickness of the wafer. See Figure 7.

7. Solder Dipping

The chip was removed from the mandrel, cleaned carefully in a solvent so as not to damage the fragile contoured edge, fluxed with a suitable flux solution and then dipped into a molten solder pot at 400°C. The composition of the solder was the ductile solder alloy selected during the R&D program for reliability under thermal fatigue conditions. This sudden thermal shock to the wafer also tests the adherence and the integrity of the metallizing.

Each chip was held and stored in a cabinet by clamping at the center in a cross-locking tweezer. This tweezer was used throughout the entire masking and etching operations. Careful handling was required because the high voltage blocking junction of the chip would be severely degraded if the fragile contoured edge should be accidentally bumped or chipped.

8. Chemical Etching of the Junction

Prior to inserting the chip into the chemical etchants, which are used to etch the exposed silicon junction, each chip was hand painted with wax. This is the only successful method, to date, for protecting the metallizing from attack by the chemicals used. When the solvents in the wax are evaporated, the chip can then be etched.

The chips were etched on the contoured edge by two, separate, brief dips into a simmering solution of hydroxide. After rinsing, the metallized surfaces of the chips were coated with wax and etched in a solution for a short time period.

9. Electrical Quality Testing of the Chip

After etching, the protective wax was removed from the chip with solvents to enable the electrical quality testing of the wafer to be performed. A chip that fails this electrical test was reprocessed through the wax masking operation and re-etched.

A demountable, insulated fixture was used to contact both sides of each chip. The electrical testing consists of a measurement of the reverse blocking capability by using a type 575 Transistor Curve Tracer. Chips which exhibit a very low value of reverse leakage current at 800 volts peak were candidates for soldering between the heat-pipes.

10. Heat-Pipe Assembly

The heat-pipe assemblies include the ceramic insulator assembly as well as the weld ring parts for the final closure of the rectifier envelope. Exhaust tubulations are included to facilitate the exhaust protubulations are included to facilitate the exhaust processing and the back-filling of the three operating chambers of the completely assembled Transcalent device. Refer to Figure 11 for a flow diagram of the various heat-pipe assembly and processing steps.

a. Heat-Pipe Design features

The proposed heat-pipe design for the J15401 Transcalent rectifier incorporates all of the design changes which RCA has developed and which have enhanced the operating characteristics and lowered the fabrication costs since the completion of the R&D Contract No. DAAK02-69-C-0609. Small diameter fins of the Wolverine tubing variety were utilized to minimize size and weight.

The discussion which follows will outline the method of fabrication while discussing the reasoning which has led to the design refinements.

Wolverine tubing is fabricated from a phosphorous deoxidized copper and is not commercially available in OFHC copper. OFHC copper can be successfully brazed in thin sections in a hydrogen atmosphere. However, if a thin section of the Wolverine tubing was brazed to the molybdenum disc, the phosphorus would lower the melting point of the gold-copper brazing alloy and holes would be dissolved in the thin wall of the tubing. This brazing problem did not occur during the R&D contract because the molybdenum disc had not yet been utilized to improve other heat-pipe characteristics.

Thus, the heat-pipe outer wall was made in two parts. One section of the heat-pipe wall was fabricated from Wolverine Tube Division, Universal Oil Products Company, Trufin tubing. This tubing has fins that are an integral part of the copper tubing wall and, therefore, have an excellent thermal efficiency (greater than 95%). The dimensions of the fins conform to those in the drawing of Figure 1.

b. Pre-Fabricated Heat-Pipes

The two heat-pipes to be used for the double-sided cooling of the rectifier chip have been further refined since the R&D contract by the addition of a thin molybdenum diaphragm or disc brazed into one end of each heat-pipe. Refer to Figure 8. The thickness of the disc is optimized for low thermal resistance as well as for the heat-sinking of high current surges without burn-out. Besides this advantage, the use of the molybdenum disc produces a prefabricated heat-pipe assembly having the following advantages over the R&D method of constructing the heat-pipe with an open end to be soldered to the silicon chip. The heat-pipes fabricated during the R&D Contract DAAK02-69-C-0609 were hermetically sealed only by a solder fillet between the silicon chip and the ends of the heat-pipes.

REVISIONS

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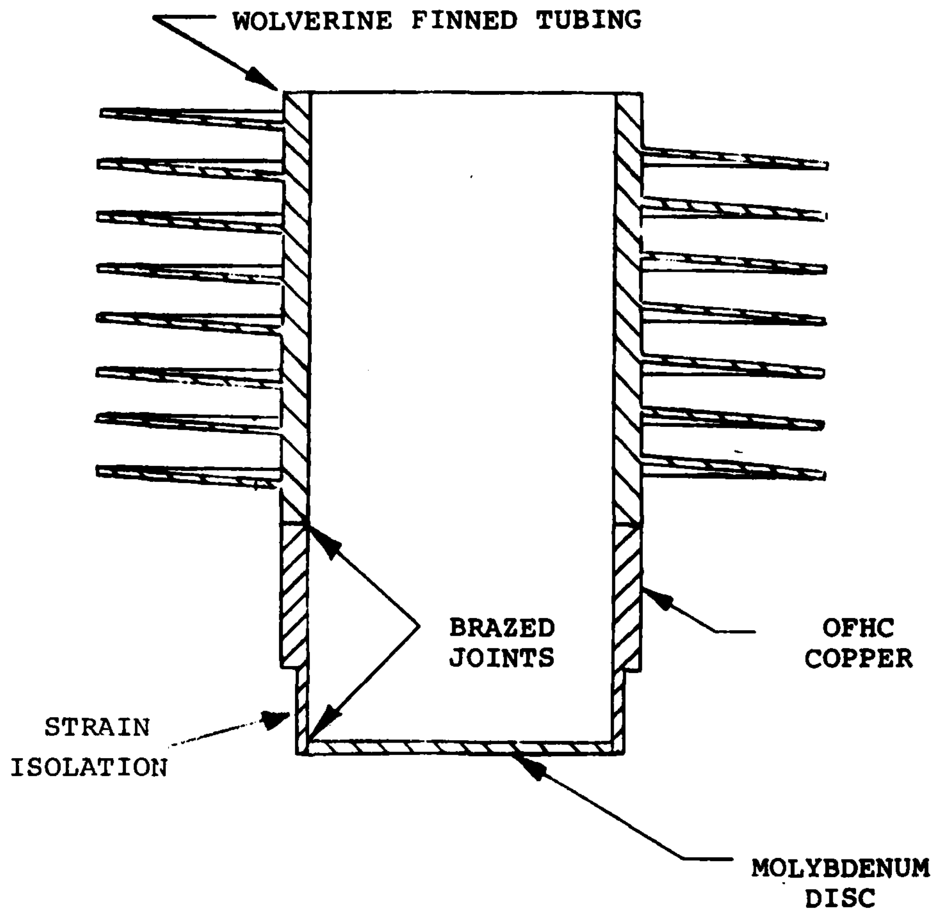


Fig. 8

TOLERANCES AND WORKMANSHIP REQUIREMENTS NOT SPECIFIED ON THIS DRAWING SHALL CONFORM TO SPECIFICATION 93650.

BASIC DIMENSIONS	2 PLACE DECIMALS	3 PLACE DECIMALS

RCA

RCA CORPORATION

CATHODE SUB-ASSLY.

DRAWN BY W. T. BURKINS

DESIGNED BY S. W. KESSLER

CHECKED BY B. B. ADAMS

In the pre-fabricated design, the joint of the heat-pipe to the metallized silicon will no longer be the fragile joint of the solder fillet between the heat-pipe and the silicon. This fillet frequently developed a leak during operation of the experimental devices.

The molybdenum sealed heat-pipe was vacuum leak checked prior to assembling it to the silicon chip. This copper-to-molybdenum brazed joint is very strong, thus, the sealed end of the heat-pipe will not be likely to develop a leak which would ruin the device during operation. By transferring the leak checking to an earlier stage of assembly, the value of the parts which must be scrapped will be greatly reduced if an occasional leak occurs. Batch or continuous furnace prebrazing of the pre-fabricated heat-pipe subassemblies will also be possible.

It has been demonstrated experimentally and under Contract DAAB07-76-C-8120 that an assembly using the molybdenum disc is very reliable and the heat-pipe is almost immune to thermal fatigue. A J15372 Transcalent thyristor of this design, but with much larger fins, has successfully passed 70,000 "on-off" cycles of 10 minutes "on" and 10 minutes "off" at the full rated current (400 A RMS). The accumulated "on time" for this device was 11,667 hours of operation without degrading of the thermal or electrical characteristics.

11. Lapping the Molybdenum Disc

The end of the heat-pipe containing the molybdenum disc is lapped flat after the sintering and brazing operations. Although the disc is initially flat, the differential expansion of the materials causes the disc to become convex after the various temperature cycles necessary to completely fabricate and wick the heat-pipe subassembly. To restore the flatness of the molybdenum disc, the heat-pipe was previously hand lapped on a flat plate.

The lapping problem was resolved through the purchase of a planetary gear lapping machine. The equipment has automatic lapping compound dispensing equipment, variable speed drive for slow start-up, and a speed adjusting control. Lapping procedures were reduced to simple load and unload operations. In addition, the lapping process does not require operator monitoring, thus, freeing the operator for other duties. Lapping quality has been improved as the process produces flatter molybdenum discs than the previous method.

Special gear shaped lapping carriers were designed to fit the machine. The design must ensure that the work traverses and touches all the boundaries of the lapping plate to prevent uneven wear of the plate. Five carriers were utilized on the equipment at one time each holding four heat-pipes. Since the lapping cycle lasted two hours, the production rate was ten lapped units per hour.

The lapping machine has been installed in a production area which is clean and presents a proper environment for good lapping procedures. The lapping machine with five carriers can be seen in Figure 9. One carrier is loaded with anode heat-pipe assemblies.

12. High Strength Wick

The next operation in the fabrication of the heat-pipes was the casting and sintering of the powder wick for the capillary return of the working fluid. It was desirable that the wick be sintered without any alloying. Metals which alloy or are sometimes added to aid sintering lower the thermal conductivity of the wick. Tapered stainless steel mandrels were used to form the inside contour of the wick while the outside dimensions of the wick were those of the inside diameter of the heat-pipe. The wick sintered itself to the inside wall of the heat-pipe and also sintered to the nickel and copper platings on the molybdenum disc. The same operation sintered the powder particles together to form a high strength, continuous, porous lining. This process formed an excellent thermal bond.

The Transcalent rectifiers fabricated during the R&D contract used a solder plated wick powder which was sintered in place after the heat-pipe was soldered to the silicon chip. A relatively low strength, porous wick resulted. In operation, the high forward current had to be conducted by this solder plated wick from the wall of the heat-pipe to the center

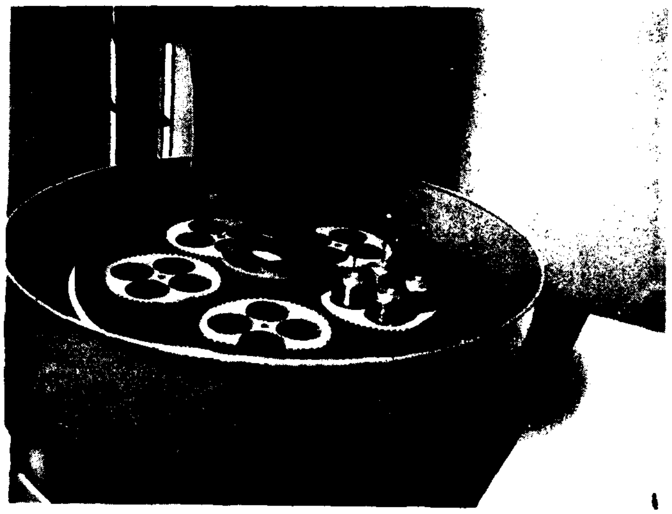


Fig. 9 Lapping Machine

of the silicon chip because only a small cross-section of the heat-pipe was joined to the silicon. This design forced a high current density at the points of contact between the particles of the wick and caused the wick, in time, to disintegrate. The disintegration increased the forward voltage drop across the rectifier. This high forward drop could lead to excess junction temperature or to a premature fatigue failure.

In the MM&T devices, with the heat-pipe closed with the molybdenum disc, the high current is conducted to the center of the silicon wafer by the high conductivity molybdenum disc adjacent to the silicon on both sides.

A high temperature braze was used to join the molybdenum disc into the end of the copper heat-pipe. This high temperature braze then enabled the designer to select intermediate temperatures for the following operations. For example, the wick is now sintered at a moderately high temperature that will allow RCA to use pure copper powder for the high strength wick material. Pure copper also has a greater thermal and electrical conductivity than the solder plated or alloy which previously used and sintered at lower temperatures.

Other advantages are that pure copper is less costly, results in a lower thermal impedance, and the thermal conductivity of the copper does not degrade with time. It is compatible with the working fluid (high purity water) to be used in the wick. A wick sintered at intermediate to high temperature will not only be mechanically stronger, but also it will be more capable of withstanding the frozen starts required by the MM&T specification.

The material which will be the greatest contributor to the thermal impedance of the J15401 rectifier will be this wick structure. The thermal properties of the wick are dependent upon its density, thus, wicks of greater densities will have greater thermal conductivities. Wick material was sintered into a rod shape and used as a test specimen to measure density and thermal conductivity. The thermal conductivity was 21% of pure copper and the density was 65% of copper.

13. Other Transcalent Envelope Parts

After sintering the wick, the ceramic to metal seal assembly was brazed to the emitter heat-pipe and a flange was brazed to the collector heat-pipe. The final braze made on the heat-pipes was performed to close the outer end of each heat-pipe with a cap that was internally threaded for the 3/8 inch stud connection. The exhaust tube was brazed into the cap prior to this assembly. Each heat-pipe assembly was helium leak checked and pinched off while under vacuum on the leak detector to prevent any foreign matter from entering the heat-pipes accidentally. The pinch-offs were reopened after final assembly for the exhaust processing and back-filling operations.

a. Stud

Salt spray tests revealed that several of the materials used in plating the studs were inadequate. Zinc plating resulted in too many white corrosion products after the salt spray test, while nickel plating resulted in excessive rust. The final solution to the problem was solved by using cadmium plating followed by a yellow chromate coating. It was concluded that the latter combination was highly tolerant of the salt spray test, since the studs looked identical before and after this test.

b. Parts Machining Refinements

Several key parts used in Transcalent subassemblies were too costly and had quality problems associated with them. The strain isolation rings suffered from a variable wall thickness when machined via normal lathe procedures. However, automatic screw machine procedures, in which both inside and outside diameters were formed at the same time, resolved this problem. Quality and cost improvements were also noted on the Wolverine finned tubing and the end caps.

c. Low Temperature Environment Solution

Figure 10 shows the cathode heat-pipe with a convoluted strain isolation ring. This convolution provides a safety factor in the event aixal stresses are imposed on the wafer at low temperatures. Experiments have revealed that differential expansion between the outside case and the center column of the device could place the wafer in tension at low temperatures of -25°C or below. The convolution provides a weak member which will flex under tension and protect the wafer. Since there were no failures in the low temperature tests required on the program, (see Environmental Testing) the concept was proven adequate for -25°C environments.

14. Rectifier Assembly and Processing

The pre-fabricated heat-pipes, a pretested silicon chip, and a weld ring are now ready to be assembled into a rectifier. A flow diagram of the assembly and processing are shown in Figure 11.

a. Soldering Chip to Heat-Pipe

The previous method of soldering the chip to the heat-pipe required a great deal of operator skill. To de-skill this assembly operation, a two-part demountable fixture was fabricated for fixturing the rectifier subassemblies.

The fixture was split so that it could easily be removed from the soldered assembly. Three concentric surfaces were included for positioning the three subassemblies. The two smallest concentric surfaces fixtured the two heat-pipes. The center cylindrical surface was made slightly larger than the largest chip. With these dimensions, the small space between the fixture and the edge of the chip without was used to gauge the alignment of the chip without the edge of the fixture coming in contact with the high voltage, contoured edge of the chip.

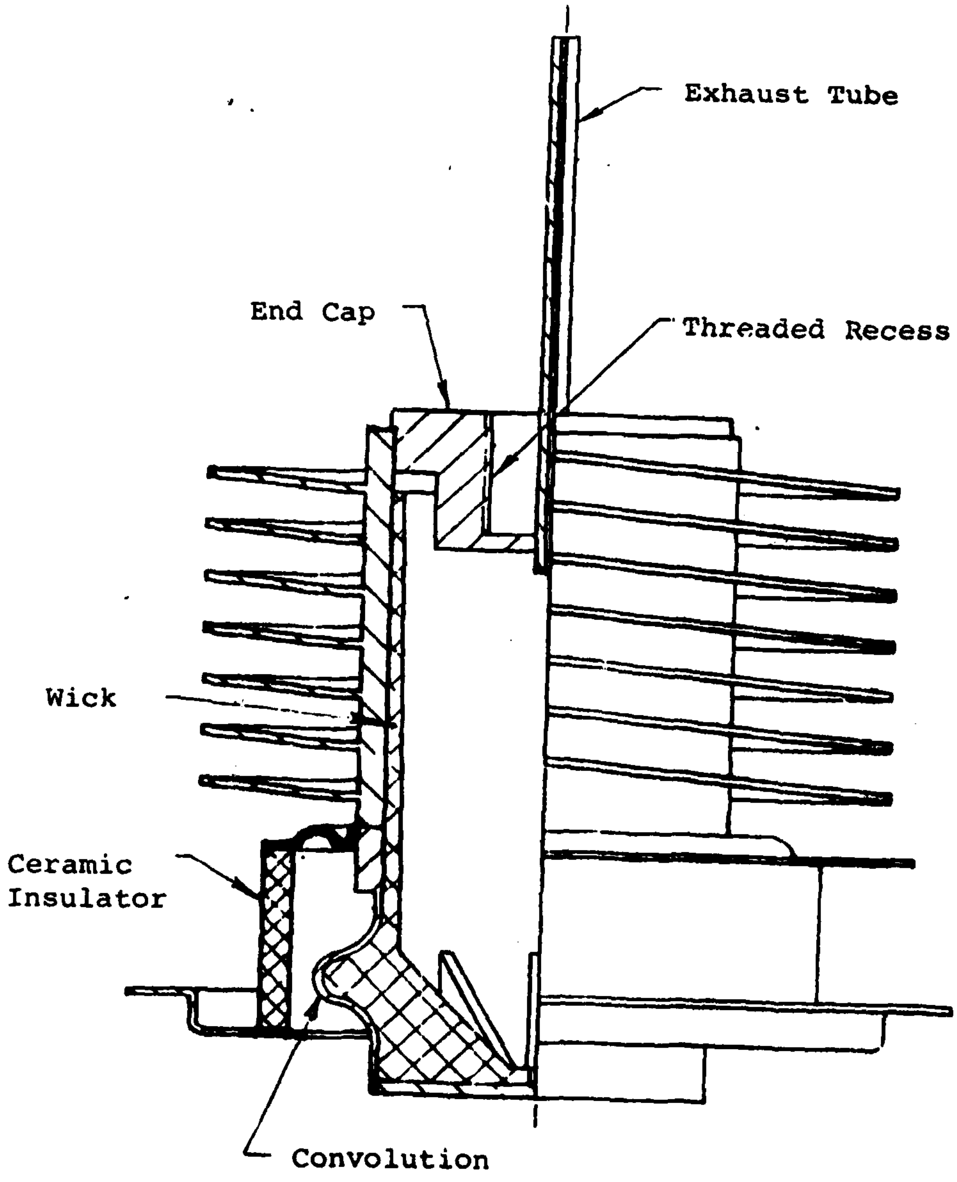


Figure 10 Pre-Fabricated Cathode (Emitter) Heat-Pipe

FLOW DIAGRAM FOR THE ASSEMBLY AND PROCESSING OF J15401

Plated Anode Heat-Pipe

Weld Ring

Processed Silioon Chip

Plated Cathode Heat-Pipe

Solder Silicon Chip Between Heat-Pipes

Passivate Edge of Chip and Cure

Weld Ring to Flanges

Exhaust and Bake Heat-Pipes and High Voltage Chamber

Dry Nitrogen

Pinch-Off Heat-Pipes and Back-Fill High Voltage Chamber with N_2

Distill Water

Distill Water Under Vacuum

Back-Fill Heat-Pipes with H_2O and Pinch-Off

Finishing Operations

Electrical, Mechanical, Thermal and Environmental Testing

Marking, Packaging and Delivery

Figure 11

A weight was added to the stacked sub-assemblies to squeeze out any excess solder in the joints. This weight prevented an excess of solder and a lack of flatness between the wafer and the discs of the heat-pipes which could increase the thermal impedance of the rectifier and lead to a weaker joint.

The devices were soldered at a partial pressure of hydrogen. The soldering was done in a furnace that RCA purchased and installed for Transcalent Devices. The furnace is capable of soldering multiple devices simultaneously. The occurrence of solder voids between chip and heat-pipes has been significantly reduced by using this procedure.

b. Heliarc Welding

The weld ring is Heliarc welded to the flanges that are attached to each heat-pipe to complete the closure of the envelope. The weld at the cathode heat-pipe has been turned 90° from the older R&D design. These are welded on a laboratory weld set-up. Each unit is carefully aligned and requires considerable skill on the part of the operator. This procedure is adequate for the confirmatory and pilot run portions of the program, however, a better procedure was investigated. If the volume of business requires it, a simple semi-automatic piece of equipment is available to de-skill this operation. Tests will be performed to simulate the set-up of the equipment being proposed. These tests will be performed during the confirmatory phase of the program and if they are successful, the equipment will be considered in future budget requests.

c. Exhaust and Back-Fill Chambers

The manifold of this RCA-owned exhaust system can exhaust six devices simultaneously.

There are three chambers to be baked out, evacuated and back-filled. The center chamber was baked and exhausted to a high vacuum and back-filled with Nitrogen.

The heat-pipes are subsequently exhausted and backfilled using a three-way valve on another vacuum system. A measured amount of high purity, distilled water is used. The amount will be that which just fills the wick structure without any excess liquid to slosh inside the heat-pipes.

The latter method of back-filling the heat-pipes with water was developed after the R&D contract was completed. The technique employs a three-way valve in which the heat-pipe exhaust tubes may be opened alternately between the vacuum system of a leak detector and pipettes filled with distilled water. The valve is used to exhaust and leak check each heat-pipe before it is back-filled with a carefully measured amount of water.

d. Finishing Operations

The completed rectifier devices were electroplated with nickel and conformal coated to protect some of the surfaces from corrosion and to improve the reduced barometric pressure operations. A label including the manufacturer's identification, device number and serial number was attached prior to the conformal coating.

The plating used on the studs mounted on each end of the device was developed to comply with salt spray requirements.

e. Detail

Additional rectifier assembly and processing details are found in the Preliminary Pilot Run Report (Sequence No. A006) and General Report on Step II (Sequence No. A007), DD1423, contract number DAAK70-78-C-0120 dated June 1980.

15. Physical Inspection

All of the critical dimensions of the five engineering samples were measured via micrometers. The resulting measurements were then compared to the limits shown on the outline drawing, Figure 1 of the MERADCOM, Semiconductor Device, Silicon Transcalent Rectifier, dated 6 June 1978. The labor

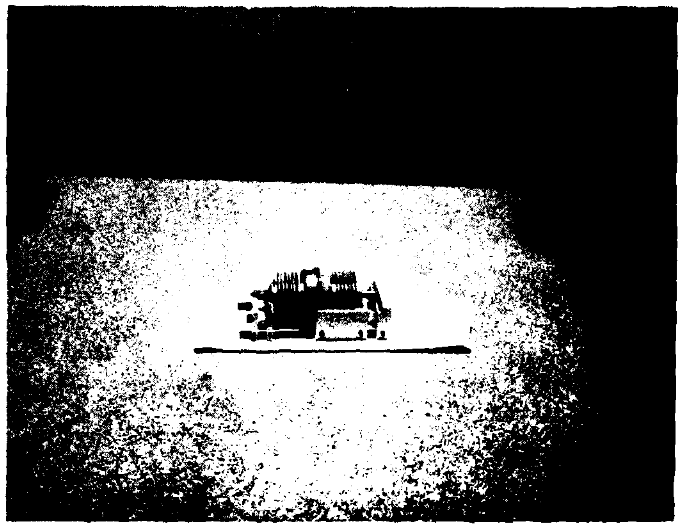


Fig. 12 J15401 "Go-No-Go" Gauge

intensity of this operation was reduced through the use of a "go-no-go" gauge shown in Figure 12. It was used in the confirmatory sample portion of the piogram.

The gauge was made to dimensions indicated in Table 2 - Physical Dimensions and was designed to check the devices within the limits of dimensions B, C, F and D, see Figure 1. No measuring tools other than the gauge were required to determine if a device was within mechanical dimensional specifications. The procedure required little experience and little time to complete. The labor intensity of the operation has been removed and the gauge is practical for production inspection. The gauge will be maintained with proper gauge care and measured periodically in the Gauge Lab as called out via computer flagging procedures.

B. Confirmatory Phase

Ten confirmatory sample rectifiers were fabricated during this phase of the contract. Four product design variations were tested in the confirmatory sample phase. However, the differences were slight as the outline or interface surfaces of the device remained the same and the performance characteristics were identical. Each variation was included as a possible production improvement consisting of the following items.

1. Ion Implantation

Two units were successfully tested which were ion implanted with a boron $N_{dose} = 6 \times 10^{15}$ at 200 KeV on one side and a phosphorus $N_{dose} = 6.5 \times 10^{15}$ at 180 KeV on the other side. There was no detectable difference in electrical performance of the ion implanted vs. the standard process rectifiers. Ion implantation eliminated five of the nine process steps and substituted the two implants.

The ion implantation was investigated as a future production method. Unfortuantely, the time for implanting with our equipment was 20 minutes per wafer for the boron side alone.

One side of a wafer could be boron doped in 3.5 minutes with our standard procedures, and this time could easily be cut in half by doubling the wafer boat size. A hot source implanter could implant economically, but the contractor does not intend to buy one at the present time. Consequently, if a pilot run had taken place, standard doped wafers would have been used.

2. Webless Wicked

RCA made experimental wicks by pressing the pre-sintered copper powder in the evaporator. Tooling was fabricated to press the wick. This design eliminates the webs presently utilized in the evaporator area. A wick of greater density was measured and compared with the thermal impedance of devices built by the present method. This concept is shown in Figure 13. The anode portion of the cross section shows a webless wick. Conversely the cathode portion (ceramic side) displays a webbed wicked assembly. Eliminating the wick is a definite process improvement which helps to make the device more manufacturable. Consequently, this approach should be used in any future production.

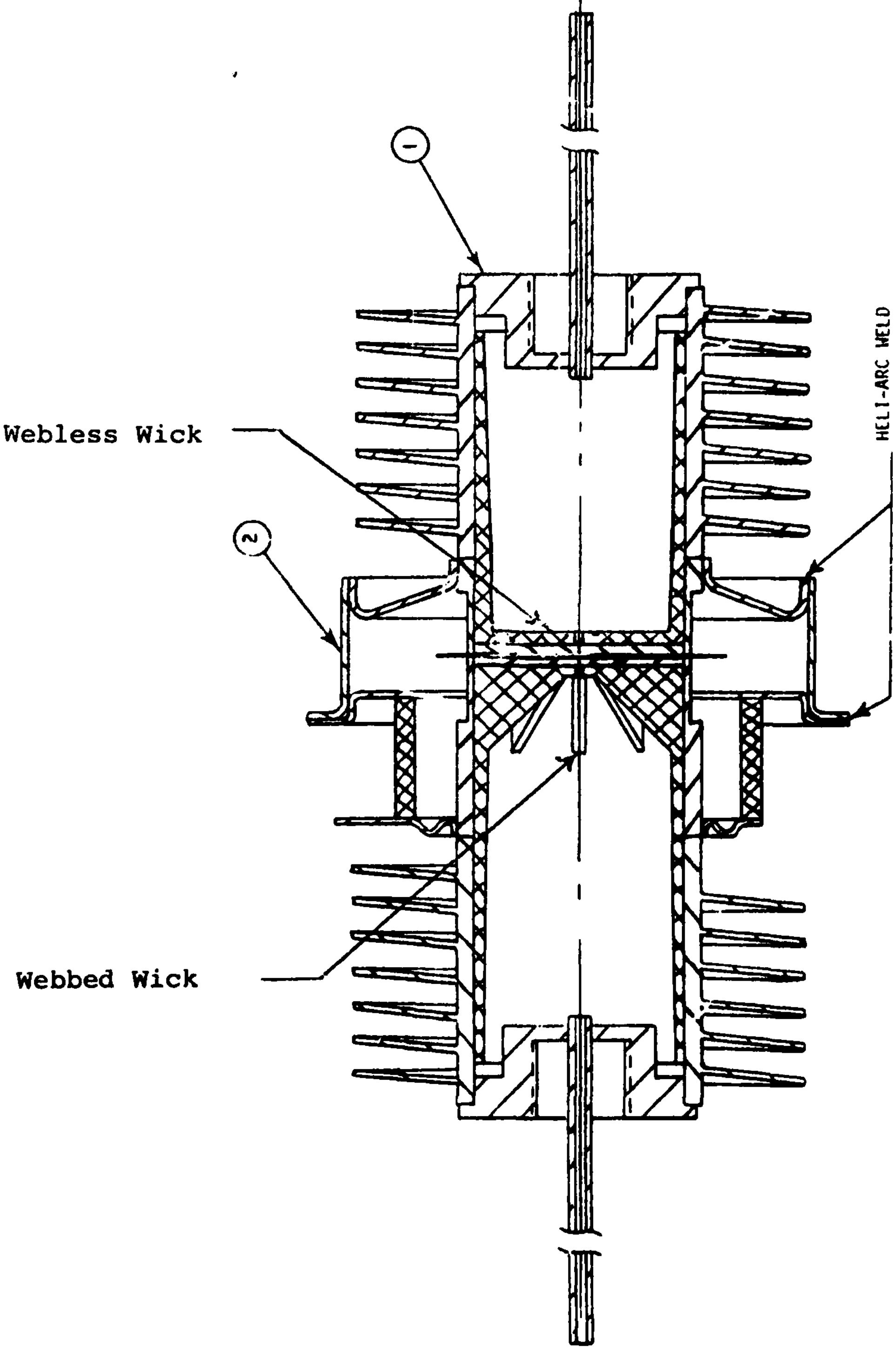
3. Tungsten Button-Convoluted

The convoluted design was incorporated into the cathode heat-pipe to reduce low temperature stresses. Figure 14 displays the convoluted concept. Test results indicate that the rectifier does not need the convolution at low temperatures which simplifies the construction of the part in question. Confidence was gained when two non-convoluted designs were tested down to $-55^{\circ}C$ which is much more severe than the $-25^{\circ}C$ test stipulated by the contract.

4. Tungsten Button - Nonconvoluted

This approach which can be seen in Figure 13 has been adopted as the pilot run design for reasons discussed under 3.

Fig. 13 Cross Section Showing Webless Wick



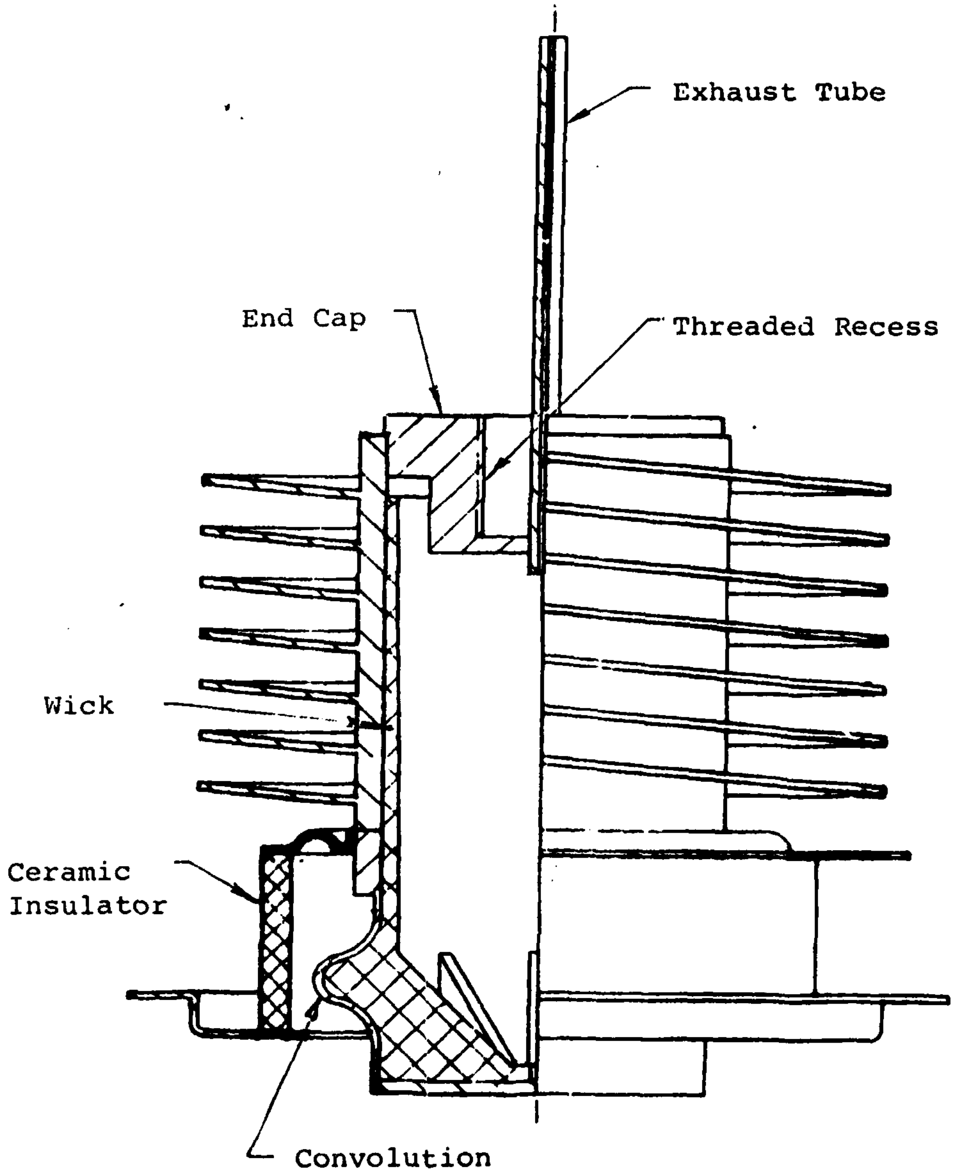


Figure 14 Pre-Fabricated Cathode (Emitter) Heat-Pipe Showing Convoluted Stress Relief

5. Conclusion

The design of any devices manufactured by future contractors should include the outline of Figure 1, standard doped wafers, webless wicks, and non-convoluted cathode strain sleeves. This combination of features has been proven acceptable via the confirmatory tests and they will remain in force as part of the identity of the J15401 Transcalent Silicon rectifier.

IV. Electrical, Mechanical, Thermal and Environmental Inspection

A. Engineering Phase

1. Group A Inspection

a. Subgroup 1

All of the Transcalent rectifiers were visually and mechanically inspected in conformance to method 2071 and Figure 1 of the specification. The dimensions of the Transcalent rectifiers were measured and recorded to verify that they conform to those of Figure 1, of the specification, using the specified method 2066.

To establish realistic tolerances for the dimensions, the actual measurements of the five engineering J15401 rectifiers are listed in Table 1 and analyzed statistically in Table 2. This analysis indicated that while all samples passed the dimensions with the tolerances listed in Figure 2 of DP-8135 (proposal for Manufacturing Methods and Technology for Silicon Transcalent Rectifier), a statistical analysis of the measured data plus fifty SCRs from a previous contract indicated some changes are necessary for the base line dimension.[1] The proposed specifications for dimensions are listed in Table 2.

b. Subgroup 2 - Test Temperature $T_A = 25 \pm 3^{o}C$

All engineering samples were tested for reverse current, i_r, and reverse voltage, v_r, under the conditions specified for method 4016.2. Figure 15 is a graph of

[1] Silicon Transcalent Thyristor, Contract No. DAAB07-76-C-8120.

TABLE 1

Meas.	F132	F133	F134	F135	F136
A	4.868	4.765	4.895	4.764	4.755
B	3.462	3.430	3.450	3.456	3.45
C	0.642	0.645	0.650	0.639	0.656
D	1.823	1.825	1.827	1.810	1.815
F	2.119	2.195	2.100	2.100	2.100

Physical Dimensions Table

TABLE 2

Sample 5 (Units measured in inches.)

		A	B	C	D	F
Spec Limits: (Using DP Outline)	Max.	5.00	3.475	0.700	1.857	—
	Nom.	--	3.450	0.650	—	2.250
	Min.	--	3.425	0.600	--	--
Recorded:	Max.	4.895	3.462	0.656	1.827	2.195
	Min.	4.764	3.43	0.639	1.810	2.100
	$\bar{x}$	4.8134	3.4496	0.6464	1.820	2.1228
	σ	0.05638	0.0176	0.0060	0.006	0.0368
	3σ	0.16914	0.0528	0.0180	0.018	0.1104
	$\bar{x} + 3\sigma$	4.983	3.5024	0.6644	1.838	2.2332
	$\bar{x} - 3\sigma$	4.644	3.3968	0.6284	1.802	2.0124
Proposed Spec. Limits	Max.	5.00	3.50	0.720	1.91	--
	Nom.	--	--	--	--	2.250
	Min.	—	3.4	0.580	--	—

J15401 Physical Dimensions
Statistical Analysis

Reverse Current +25°C

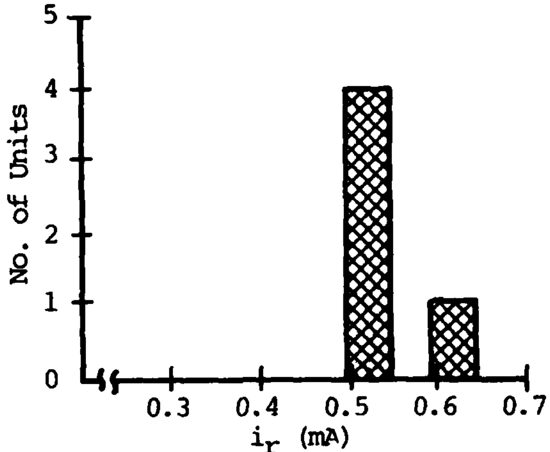


Fig. 15

Reverse Current +125°C

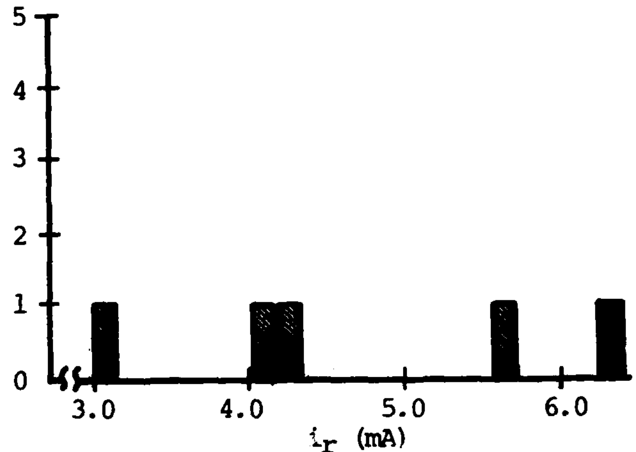


Fig. 16

Forward Voltage Drop

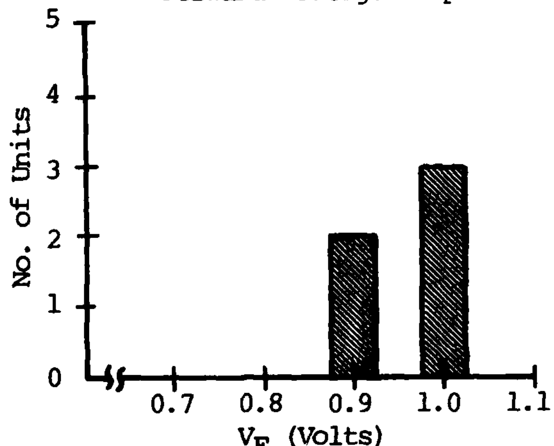


Fig. 17

Thermal Impedance

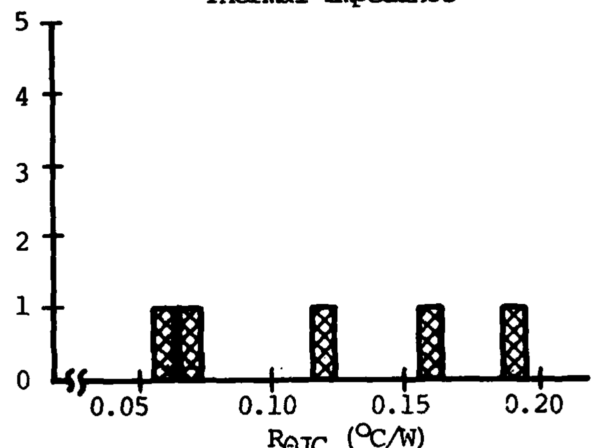


Fig. 18

Reverse Current Post Surge

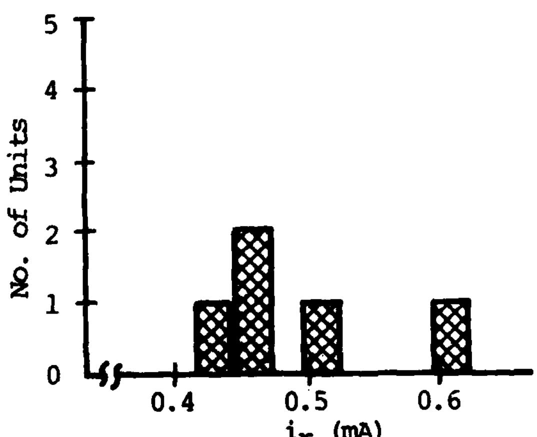


Fig. 19

Reverse Recovery Time

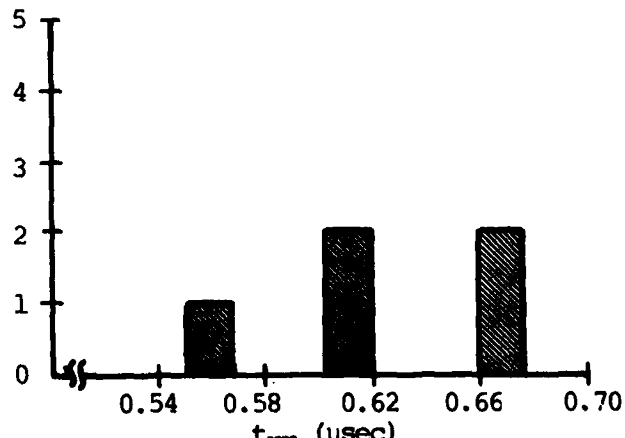


Fig. 20

the reverse current measured under the conditions in the specification. Table 3 lists the detail data.

Prior to submitting the devices to electrical test they all were tested out to 1000 volts of reverse voltage to insure that a sufficient safety margin existed.

c. Subgroup 3 - Thermal Resistance

The thermal resistance of the Transcalent rectifiers was measured using the specified method described in paragraph 4.6.1 of the specification. Each rectifier was calibrated for a temperature dependent parameter by recording the forward voltage drop at 4 amperes at several temperatures. The thermal resistance ($R_{\theta JC}$) was tested at 250 amperes of heating current, interrupted by a short period of time (less than 1 msec.) when the current was reduced to the metering value of 4 amperes. The forward voltage drop across the device was measured and used to determine the junction temperature from the calibration data. Simultaneously, the external temperature of the heat-pipes was measured and recorded. The difference in temperatures divided by the input heating power is the thermal impedance (transient) or resistance (steady state) of the device. The values of thermal resistance calculated from the data measured on the five engineering samples are shown in Table 3. Figure 18 is a graph of these data. Thermal resistance calculated on the same devices after the environmental tests are listed in Table 4 with the initial values for comparison.

d. Subgroup 4 - Test Temperature of Case: $125 \pm 6^{\circ}C$ Reverse Current, i_r, and Reverse Voltage, v_r

The devices were tested under the specified conditions by method 4016.2. The peak current max. is 60mA. The detail data measured is listed in Table 3. Figure 16 is a graph of the distribution of the i_r measured at a reverse voltage of 800 V. These data indicate that all the devices were well within the maximum limits specified.

TABLE 3

Date 10/25/78

Tester P. Bransby

Engineering Samples

Electrical Data

	Visual	Dimensions	+25°C Rev. Cur. and Rev. Voltage	Thermal Resistance for Rect. Diode	+125°C Rev. Current and Rev. Voltage	Forward Voltage	Post Surge Current Test	Reverse Recovery Time	Post Barometric Pressure
Method	2071	2066	4016.2	Para. 4.6.1	4016.2	4011.3	4066.2	4031	1001.1
Symbol			i_r	$R_{\theta JC}$	i_r	V_F	i_r	t_{rr}	i_r
Units			mA	°C/W	mA	Volts	mA	usec.	mA
Ser. No.									
F132	✓	✓	0.51	0.07	5.77	0.9	0.46	2.8	0.61
F133	✓	✓	0.51	0.06	3.09	0.9	0.51	2.7	0.61
F134	✓	✓	0.51	0.12	6.39	1.0	0.61	2.7	0.67
F135	✓	✓	0.51	0.19	4.12	1.0	0.43	2.8	0.56
F136	✓	✓	0.61	0.16	4.32	1.0	0.46	2.9	0.67
Spec.			15 Max.	0.2 Max.	60 Max.	2.0 Max.	15 Max.	15.0 Max.	15 Max.

2. Group B Inspection

a. Subgroup 1 - Forward Voltage, V_f: Test at Room Ambient Temperature of 25 ± 3°C

The peak forward voltage drop was measured across all of the devices using method 4011.3. The devices were conducting an average current of 250 amperes when the measurements were made. Since the current conducted by the device is nearly 180° of conduction angle, the peak current is approximately 800 amperes and the RMS current is about 400 amperes.

During the tests, the Transcalent rectifiers were allowed to reach thermal equilibrium and the heat-pipe was confirmed to be isothermal. Room ambient air was blown across the fins to limit the temperature of the heat-pipes to 100°C.

The individual data are listed in TABLE 3 and the distribution is shown in Figure 17. All devices passed.

b. Subgroup 2 - Surge Current, i_f Test Temperature, T_A = 25 ± 3°C

All engineering samples were tested under the conditions listed in the specification using method 4066.2. The surge current test was performed in the RCA-owned test circuit that was developed for the J15371 Transcalent thyristor under Contract No. DAAB07-76-C-8120 and modified to test the rectifiers. The pulses of surge current were repeated at a rate of one pulse per minute for ten total surges. The 800 volts of reverse voltage, V_r, was reapplied following each surge. After the surge test, the reverse current was remeasured to confirm that the 4000 amperes peak surge currents did not damage the devices.

The values of reverse current measured after this surge test are listed in Table 3 and the distribution is plotted in Figure 19. Comparing these data with those measured initially (reverse current - 25°C) indicated the engineering samples were not affected by the surge test.

c. Subgroup 3 - Reverse Recovery Time, T_{rr}
Test Temperature $T_A = 25 \pm 3^oC$

All devices were tested for reverse recovery time per the procedures of method 4031 of MIL-Std-750B. A modified circuit as outlined in the JEDEC Publication No. RS282 was used. This circuit utilizes the circuit parameters specified, however, the I_{FM} is standardized at 125 instead of 50 peak amperes.

The data measured on the engineering samples are listed in Table 3 and the distribution shown in Figure 20. Again, the devices passed with margin.

3. Group C Inspection

a. Subgroup 1 - Barometric Pressure Reduced

All of the engineering devices were successfully tested under the conditions listed using the specified method 1001.1. A device which arcs over or exhibits harmful coronas that deteriorate the device is considered a failure. After exposure to the low pressure test the devices were tested for reverse current per Subgroup 2 of Table 1. The detail data is listed in Table 3 and the distribution plotted in Figure 21.

b. Subgroup 2 - Blocking Voltage Life Test
Temperature: $T_C = 125 \pm 6^oC$

All of the engineering devices were rested for 200 hours, each under the conditions specified, using the method of para. 4.6.2. After exposure to the blocking voltage life test, the reverse current was measured and recorded. The detail data measured is listed in Table 4 and the distribution of the data plotted in Figure 22. All devices passed with margin.

c. Subgroup 3 - Thermal Shock and Salt
Atmosphere Test

All the engineering devices were tested for Thermal Shock using test method 1051.1 and the conditions stated in the specification. After five cycles, the rectifiers were removed from the environmental chamber and subjected to the moisture resistance test, method 1021.1.

Reverse current measurements per Subgroup 2 of Table 1 of the specifications were taken as a check at this point to determine if the device had survived the Thermal Shock and Moisture Resistance tests. All units passed. Detail data is listed in Table 4 and the distribution plotted in Figure 23.

All of the engineering models were subjected to the Salt Atmosphere test method 1041.1 for 24 hours. After the test, the salt was washed off of the devices which were then examined. The markings were legible and there was no evidence of flaking, pitting of the finish, or corrosion that would interfere with the application of the devices.

Examination of the samples indicated that while the devices passed the Moisture Resistance and Salt Atmosphere tests the mounting studs may have a potential cosmetic problem. This was resolved by evaluating an alternate plating for the studs. Tests on studs plated with cadmium with yellow cromate coating survived the Salt Atmosphere test with no cosmetic problem. (See Section 13-a for details.). The decision was made to use the new plating and now all the studs on the engineering models have been replaced with the new studs.

Reverse current tests per Subgroup 2 of Table 1 of the specification were performed, the detail data is listed in Table 4, and the distribution is plotted in Figure 24. All devices passed with margin.

d. Subgroup 4

All of the engineering samples were tested for reliability under the specified Thermal Fatigue Test conditions and Spec. paragraph 4.6.3. The "on" and "off" times were two minutes each. The air flow across the devices was adjusted so that when the devices were conducting, the case or heat-pipe temperature was 90 ± 10^{o}C max. and 30 ± 10^{o}C min. The devices were subjected to a minimum of 200 "on-off" cycles. Since two devices were tested simultaneously in an inverse parallel connection and the number of devices was odd (5), one device, Ser. No. F133, was subjected to a total of 400 cycles.

Five measurements per Subgroup 2 of Table 1 were made with detail data listed in Table 5 and the distribution plotted in Figure 26.

e. Subgroup 5

All of the engineering samples were shock tested in RCA's Environmental Laboratory, Lancaster, PA, using the specified conditions and test method 2016.2.

Following the shock tests, all devices were subjected to a vibration test of variable frequency described in the Specification and Test Method 2056.

After the shock and vibration tests, the reverse current measurement at 800 volts, and the thermal resistance measurements of Subgroups 2 and 3 of Table 1 were repeated successfully to verify the integrity of the devices. Detail data are listed in Table 5 and the distribution is plotted in Figure 25.

4. General Data

An additional Thermal Resistance Test was performed at the end of the test program to determine if this important parameter had degraded significantly as a result of the test program, however, it had not. See Table 4 for detail data and Figure 27 for the distribution. Table 5 lists the Post Environmental Data.

Table 6 lists the initial and final measurements of reverse currents ($T_c = 25 \pm 3^{o}C$) recorded during the environmental test program. No significant changes are present and Table 1 lists the maximum limits of the Physical Dimensions.

Figure 28 is a graph of the reverse current vs. case temperature of the rectifier. While

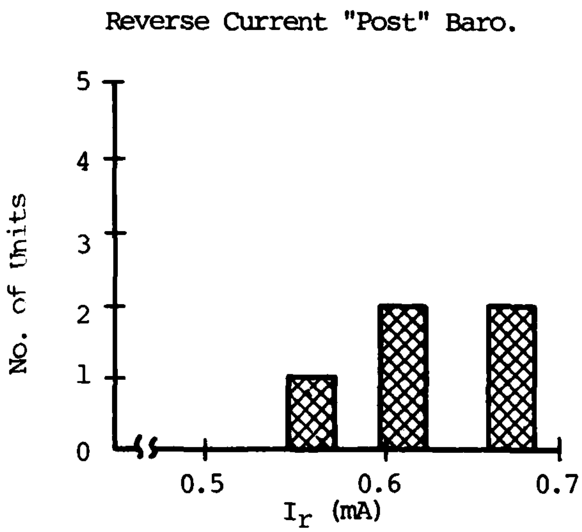


Fig. 21

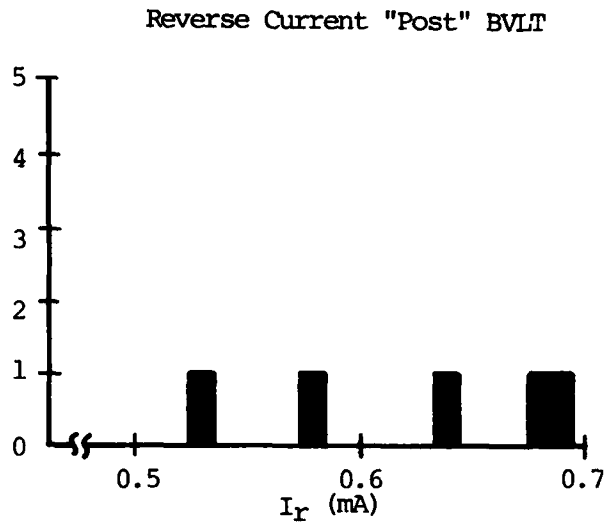


Fig. 22

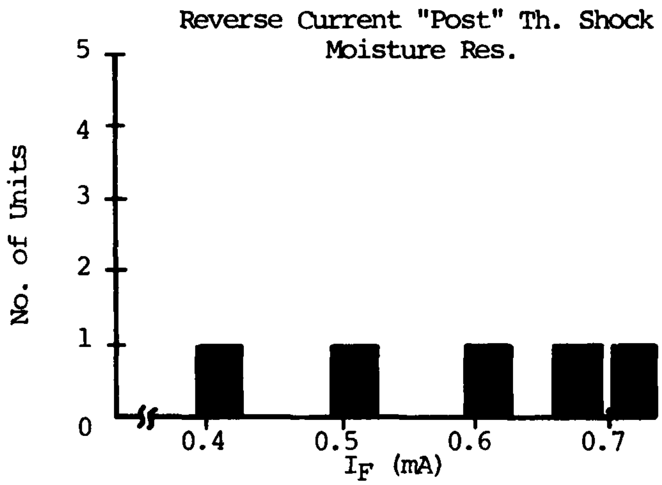


Fig. 23

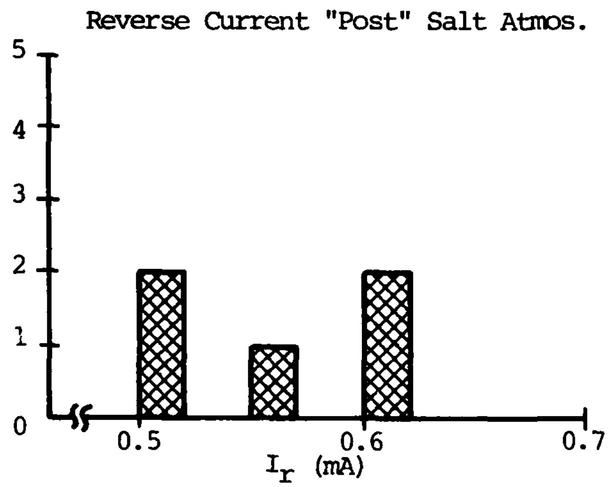


Fig. 24

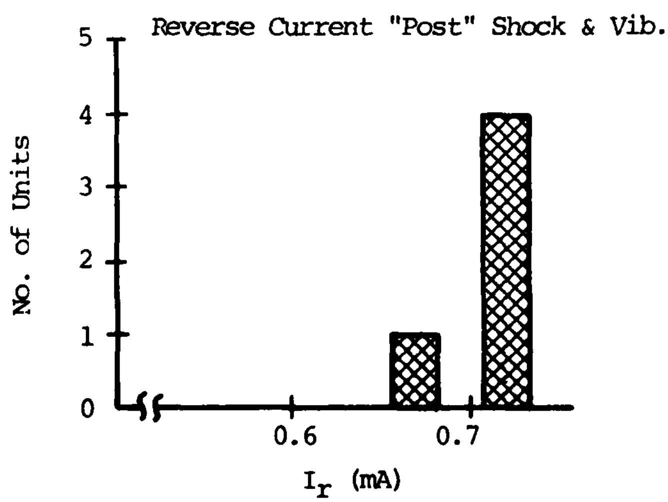


Fig. 25

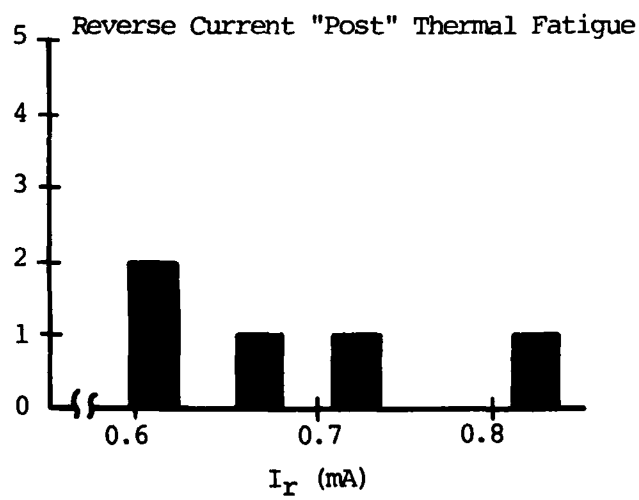


Fig. 26

TABLE 4

$T_a = 25 \pm 3^oC$

Ser. No.	F132	F133	F134	F135	F136	Max. Specification $^oC/W$
Initial	0.07	0.06	0.12	0.19	0.16	0.2
Final	0.17	0.06	0.10	0.12	0.13	0.2

Initial and Final Thermal Resistance
$^oC/W$

TABLE 5

Post Environmental Data

Date 12/20/78

Tester P.B.

	Post Blocking Voltage L.T.	Post Thermal Shock & Moisture Test	Post Salt Spray Test	Post Shock & Vibration Test	Post Thermal Fatigue L.T.	Post Envir. Thermal Resistance Test
Method	Par. 4.6.2	1051.1, 1021.1	1041.1	2016.2, 2056	Par. 4.6.3	Par. 4.6.1
Symbol Units	i_r mA	i_r mA	i_r mA	i_r mA	i_r mA	$R_{\theta JC}$ $^{o}C/W$
Serial No.						
F132	0.53	0.41	0.56	0.67	0.67	0.17
F133	0.64	0.72	0.61	0.72	0.722	0.06
F134	0.69	0.61	0.61	0.72	0.825	0.10
F135	0.58	0.67	0.51	0.72	0.61	0.12
F136	0.68	0.51	0.51	0.72	0.61	0.13
Spec.	15 (max.)	15 (max.)	15 (max.)	15 (max.)	15 (max.)	0.2 (max.)

TABLE 6

Initial and Final Measurements of Reverse Currents

$T_c = 25 \pm 3^oC$

Ser. No.	F132	F133	F134	F135	F136	Max. Speci-fication i_r(mA)
Initial	0.51	0.51	0 .51	0.51	0.51	15
Post Surge Current Test	0.46	0.51	0.61	0.43	0.46	15
Post Barometric Pres-sure Test	0.61	0.61	0 .67	0.56	0.67	15
Post Blocking Voltage Test	0.53	0.64	0 .69	0.58	0.68	15
Post Thermal Shock & Moist. Resist. Tests	0.41	0.72	0 .61	0.67	0.51	15
Post Salt Atmos. Test	0.56	0.61	0 .61	0.51	0.51	15
Post Shock & Vibration Tests	0.67	0.72	0 .72	0.72	0.72	15
Post Thermal Fatigue Test (Final Test)	0.67	0.722	0 .825	0.61	0.61	15

Final Thermal Impedance

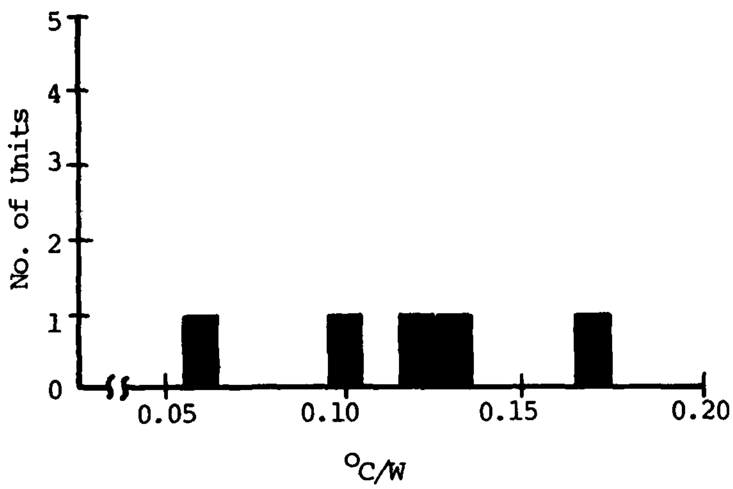


Fig. 27

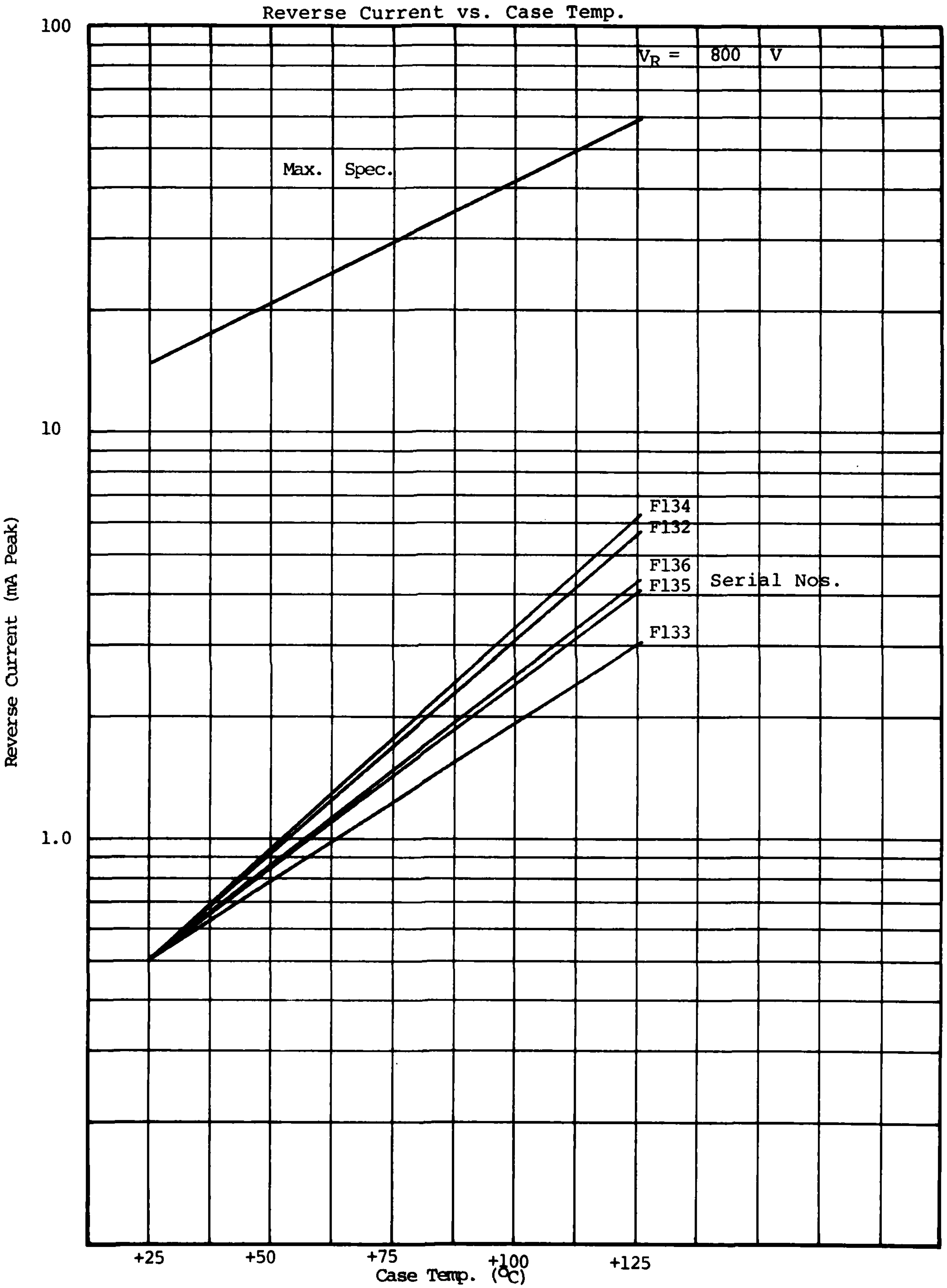

Reverse Current vs. Case Temp.
100
10
1.0
V_R = 800 V
Max. Spec.
F134
F132
F136
F135
F133
Serial Nos.
Reverse Current (mA Peak)
+25
+50
+75
+100
+125
Case Temp. (°C)

Fig. 28

reverse current increases with temperature as expected, it is sufficiently lower than the specification limit.

5. Ion Implanted Samples

Three ion implanted devices were tested. Initial tests per the specification were performed and the detail data are listed in Table 7. One of the rectifiers, Ser. No. I-1, had significant differences in its Reverse Recovery Time and Reverse Current ($T_C = 125^oC$) from the other two devices.

Ser. No.	Reverse Current (+125°C) mA	Reverse Recovery Time μSec
I-1	5.56	6.0
I-2	1.44	2.4
I-3	1.44	2.0

The cause for this difference was not determined. During the Surge Current, S/N I-1 developed a short. I-2 and I-3 appeared to have faster recovery time than the engineer-models, however, two pieces of data are not statistically significant.

B. Confirmatory Phase

Ten silicon rectifiers were tested during the Confirmatory Sample phase of this program. The procedure used was "RCA Acceptance Test Procedure (ATP) Silicon Transcalent Rectifier, J15401 dated 30 May 1979. (See appendix) The total sample consisted of four variations. The serial numbers and corresponding construction variations were as follows:

Ser. No.	Variation
II-2	Ion Implanted
II-3	
J149	Webless Wicked
J150	
J151	
J157	Tungsten Button: Convoluted
J160	
J162	
J156	Tungsten Button: Nonconvoluted
J163	

TABLE 7

Ion Implanted Samples

Electrical Data

Date 12/20/78

Tester P.B.

	Visual	Dimensions	+25°C Rev. Cur. and Rev. Voltage	Thermal Resistance for Rect. Diode	+125°C Rev. Current and Rev. Voltage	Forward Voltage	Post Surge Current Test	Reverse Recovery Time
Method Symbol	2071	2066	4016.2 i_r	Para. 4.6.1 $R_{\theta JC}$	4016.2 i_r	4011.3 V_f	4066.2 i_r	4031 t_{rr}
Units			mA	°C/W	mA	Volts	mA	usec.
Ser. No.								
1	✓	✓	0.92	0.16	5.56	1.0	*	6.0
2	✓	✓	0.61	0.10	0.14	1.0	0.61	2.4
3	✓	✓	0.92	0.20	1.44	1.0	0.67	2.0
Spec.			15 Max.	0.2 Max.	60 Max.	2.0 Max.	15 Max.	15.0 Max.

*Shorted during surge test.

Due to the variations in construction, the number of units subjected to each environmental test was equal to or greater than the sample size listed in the confirmatory test plan previously issued. Table 8 lists the plan's sample size and the actual number of devices tested. In addition, it lists the permitted percentage of failures.

1. Group A Inspection

   a. Subgroup 1

      All of the Transcalent rectifiers were visually and mechanically inspected in conformance to method 2071 and Figure 1 of the specification as modified by the Interim Engineering Report dated January 1979 using the specified method 2066. The actual measurements of the ten confirmatory J15401C rectifiers are listed in Table 9. Table 10 shows the results of a statistical analysis of these data which indicate that all of the devices met the specified dimensions with margin.

      In addition to taking actual measurements all the devices were checked using the "go-no-go" gauge shown in Figure 12.

   b. Subgroup 2 - Test Temperature $T_A = 25 \pm 3^{o}C$

      All confirmatory samples were tested for reverse current, i_r, and reverse voltage, V_r, under the conditions specified for method 4016.2. Figure 29 is a histogram of the reverse current measured under the conditions in the specification. Table 11 lists the detail data.

      From the statistical data we can expect all of the measurements to be less than 1.2 mA or 8% of the specified 15 mA maximum.

      Prior to submitting the devices to electrical test they all were tested out to 1000 volts of reverse voltage to insure that a sufficient safety margin existed.

   c. Subgroup 3 - Thermal Resistance

      The thermal resistance of the Transcalent rectifiers was measured using the specified method described in paragraph 4.6.1 of the

TABLE 8

Sample Size

Subgroup No.	Title	% of Units To Be Tested	Actual % of Units Tested	% Allowed To Fail	Actual % Failed
1	Barometric Pressure Reduced	50	100	0	0
2	Blocking Voltage L.T.	30	100	0	0
3	Thermal Shock	20	100	0	0
	Moisture Resistance	20	20	0	0
	Salt Atmosphere	20	20	0	0
4	Thermal Fatigue	100	100	10	0
5	Shock	20	50	0	0
	Vibration, Variable Freq.	20	50	0	0

Table 9

Physical Dimensions of Confirmatory Samples

Device #	A	B	C	D	F
II2	4.761	3.456	0.640	1.808	2.100
II3	4.761	3.464	0.650	1.834	2.100
J149	4.737	3.447	0.635	1.800	2.104
J150	4.751	3.463	0.647	1.806	2.101
J151	4.744	3.455	0.641	1.805	2.100
J156	4.748	3.476	0.624	1.800	2.100
J157	4.723	3.465	0.632	1.790	2.102
J160	4.749	3.472	0.631	1.792	2.106
J162	4.748	3.472	0.628	1.804	2.102
J163	4.718	3.463	0.635	1.803	2.100

Table 10

Statistical Analysis of the Dimensional Data of the Confirmatory Samples

Character	Avg.	Sigma	Max.	Min.	Chi-Sq.	N
Dim. A	4.744	0.014	4.761	4.718	8.38	10
Dim. B	3.463	0.009	3.476	3.447	2.95	10
Dim. C	0.636	0.008	0.650	0.624	3.82	10
Dim. D	1.804	0.012	1.834	1.790	12.40	10
Dim. F	2.102	0.002	2.106	2.100	15.21	10

TABLE 11

Confirmatory Samples

Electrical Data

Date 9/5/79

Tester P. Bransby

	Visual	Dimensions	+25°C Rev. Cur. and Rev. Voltage	Thermal Resistance for Rect. Diode	+125°C Rev. Current and Rev. Voltage	Forward Voltage	Post Surge Current Test	Reverse Recovery Time	Post Barometric Pressure
Method Symbol	2071	2066	4016.2 i_r	Para. 4.6.1 $R_{\theta JC}$	4016.2 i_r	4011.3 V_f	4066.2 i_r	4031 t_{rr}	1001.1 i_r
Units			mA	°C/W	mA	Volts	mA	usec.	mA
Ser. No.									
J149	✓	✓	0.81	0.10	1.75	1.0	0.72	2.8	0.72
J150	✓	✓	0.61	0.11	1.80	1.0	0.51	2.6	0.72
J151	✓	✓	0.77	0.11	4.12	1.0	0.61	2.8	0.72
J156	✓	✓	0.92	0.07	6.18	0.92	0.72	2.4	0.68
J157	✓	✓	0.92	0.09	5.36	0.98	0.82	2.9	0.72
J160	✓	✓	0.92	0.08	2.06	0.98	0.82	3.0	0.72
J162	✓	✓	0.82	0.08	2.57	1.0	0.82	3.2	0.72
J163	✓	✓	0.92	0.20	1.85	1.0	0.82	2.9	0.69
II-2	✓	✓	0.61	0.10	1.44	1.0	0.61	2.4	0.33
II-3	✓	✓	0.92	0.20	1.44	1.0	0.67	2.0	0.29
Spec.			15 Max.	0.2 Max.	60 Max.	2.0 Max.	15 Max.	15.0 Max.	15 Max.

specification. Each rectifier was calibrated for a temperature dependent parameter by recording the forward voltage drop at 4 amperes at several temperatures. The thermal resistance ($R_{\theta JC}$) was tested at 250 amperes of heating current, interrupted by a short period of time (less than 1 msec.) when the current was reduced to the metering value of 4 amperes. The forward voltage drop across the device was measured and used to determine the junction temperature from the calibration data. Simultaneously, the external temperature of the heat-pipes was measured and recorded. The difference in temperatures divided by the input heating power is the thermal impedance (transient) or resistance (steady state) of the device. The values of thermal resistance calculated from the data measured on the ten confirmatory samples are shown in Table 11. Figure 30 is a histogram of these data. Thermal resistance calculated on the same devices after the environmental tests are listed in Table 12 with the initial values for comparison.

Two of the devices, I13 (ion implanted) and J163 (nonconvoluted), had initial Thermal Impedance measurements at the upper limit of the specification, 0.2^{o}C/W. Since similarly constructed devices in the confirmatory sample, II-2 and J156, had initial normal measurements of 0.1^{o}C/W and 0.07^{o}C/W respectively, it is not believed that the high measurements are construction orientated, but rather a normal variation.

d. Subgroup 4 - Test Temperature of Case: 125 ± 6^{o}C Reverse Current, i_r, and Reverse Voltage, V_r

The devices were tested under the specified conditions by method 4016.2. The specification limit for maximum peak current is 60 mA.

```
HISTOGRAM DATA[;1]

LOWER CELL LIMIT,CELL WIDTH AND NUMBER OF CELLS :.5 .02 25
VERT SCALE:1
CHAR:IR+25  C
   CHARACTERISTIC-IR+25  C
    AVERAGE- 0.822
    SIGMA--- 0.1250599856
    MAXIMUM- 0.92
    MINIMUM- 0.61
    SAMPLE-- 10

  5+                      □
  4+                      □
  3+                      □
  2+     □                □
  1+     □       □ □□     □
   ++++++++++++++++++++++++++
    0 0 0 0 0 0 0 0 0 0 0 0 0
    . . . . . . . . . . . . .
    5 5 5 6 6 7 7 7 8 8 9 9 9
      4 8 2 6   4 8 2 6   4 8
```

Limit
15 mA Max.

No. of Devices

Fig. 29 Reverse Current at +25°C, (mA)

Histogram Data (3)

```
LOWER CELL LIMIT,CELL WIDTH AND NUMBER OF CELLS :.03 .02 25
VERT SCALE:1
CHAR:ROJC
     CHARACTERISTIC-RθJC
   AVERAGE- 0.114
   SIGMA--- 0.04718756898
   MAXIMUM- 0.2
   MINIMUM- 0.07
   SAMPLE-- 10

  4+    □
  3+   □□
  2+   □□     □
  1+  □□□     □
   ++++++++++++++++++++++++++
    0 0 0 0 0 0 0 0 0 0 0 0 0
    . . . . . . . . . . . . .
    0 0 1 1 1 2 2 3 3 3 4 4 5
    3 7 1 5 9 3 7 1 5 9 3 7 1
```

Limit
0.2° C/W

No. of Devices

Fig. 30 Thermal Resistance, $R_{\theta JC}$ ($^{\circ}$C/W)

Table 12

Initial and Final Thermal Resistance

$^{o}C/W$

$T_A = 25 \pm 3^{o}C$

Ser. No.	J149	J150	J151	J156	J157	J160	J162	J163	II2	II3	Max. Spec. $^{o}C/W$
Initial	0.1	0.11	0.11	0.07	0.09	0.08	0.08	0.2	0.1	0.2	0.2
Final	0.13	0.10	0.16	0.14	0.10	0.1	0.09	0.15	0.2	0.19	0.2

The detail data measured is listed in Table 11. Figure 31 is a histogram of the distribution of the i_r measured at a reverse voltage of 800 V. These data indicate that all the devices were well within the maximum limits specified.

2. Group B Inspection

a. Subgroup 1 - Forward Voltage, V_f: Test at Room Ambient Temperature of 25 ± 3°C

The peak forward voltage drop was measured across all of the devices using method 4011.3. The devices were conducting an average current of 250 amperes when the measurements were made. Since the current conducted by the device is nearly 180° of conduction angle, the peak current is approximately 800 amperes and the RMS current is about 400 amperes.

During the tests, the Transcalent rectifiers were allowed to reach thermal equilibrium and the heat-pipe was confirmed to be isothermal. Room ambient air was blown across the fins to limit the temperature of the heat-pipes to 100°C.

The individual data are listed in Table 11 and the distribution is shown in Figure 32. All devices passed.

b. Subgroup 2 - Surge Current, i_f Test Temperature, T_A = 25 ± 3°C

All confirmatory samples were tested under the conditions listed in the specification using method 4066.2. The surge current test was performed in the RCA owned test circuit that was developed for the J15371 Transcalent thyristor under Contract No. DAAB07-76-C-8120 and modified to test the rectifiers. The pulses of surge current were repeated at a rate of one pulse per minute for ten total surges. The 800 volts of reverse voltage, V_r, was reapplied following each surge. After the surge test, the reverse current was remeasured to confirm that the 4000 amperes peak surge currents did not damage the devices.

Histogram Data (2)

```
LOWER CELL LIMIT,CELL WIDTH AND NUMBER OF CELLS :1.0 .22 25
VERT SCALE:1
CHAR:IR+125
    CHARACTERISTIC-IR+125
    AVERAGE- 2.857
    SIGMA--- 1.731813757
    MAXIMUM- 6.18
    MINIMUM- 1.44
    SAMPLE-- 10

 2+  □ □
 1+  □□□□ □      □     □   □
  +++++++++++++++++++++++++++
    1 1 1 2 2 3 3 4 4 4 5 5 6
      . . . . . . . . . . . .
      4 8 3 7 2 6 0 5 9 4 8 2
      4 8 2 6   4 8 2 6   4 8
```

No. of Devices

Limit
60 mA Max.

Fig. 31 Reverse Current at 125°C Case Temp., (mA)

Histogram Data (4)

```
LOWER CELL LIMIT,CELL WIDTH AND NUMBER OF CELLS :.8 .01 25
VERT SCALE:1
CHAR:VFM
      CHARACTERISTIC-VFM
   AVERAGE- 0.988
   SIGMA--- 0.02529822128
   MAXIMUM- 1
   MINIMUM- 0.92
   SAMPLE-- 10

 7+                    □
 6+                    □
 5+                    □
 4+                    □
 3+                    □
 2+                  □ □
 1+            □     □ □
  +++++++++++++++++++++++++++
   0 0 0 0 0 0 0 0 0 0 1 1 1
   . . . . . . . . . .   . .
   8 8 8 8 8 9 9 9 9 9   0 0
     2 4 6 8   2 4 6 8   2 4
```

No. of Devices

Limit
2 V Max.

Fig. 32 Forward Voltage Drop, V_F (volts)

The values of reverse current measured after this surge test are listed in Table 11 and the distribution is plotted in Figure 33. Comparing these data with those measured initially (reverse current - 25°C) indicated the confirmatory samples were not affected by the surge test.

c. Subgroup 3 - Reverse Recovery Time, T_{rr}
Test Temperature $T_A = 25 \pm 3°C$

All devices were tested for reverse recovery time per the procedures of method 4031 of MIL-Std-750B. A modified circuit as outlined in the JEDEC Publication No. RS282 was used. This circuit utilizes the circuit parameters specified, however, the I_{FM} is standardized at 125 instead of 50 peak amperes.

The data measured on the engineering samples are listed in Table 11 and the distribution shown in Figure 34. Again, the devices passed with margin.

3. Group C Inspection

a. Subgroup 1 - Barometric Pressure Reduced

All of the confirmatory devices were successfully tested under the conditions listed using the specified method 1001.1. A device which arcs over or exhibits harmful coronas that deteriorate the device is considered a failure. After exposure to the low pressure test the devices were tested for reverse current per Subgroup 2 of Table 1. The detail data is listed in Table 11 and the distribution plotted in Figure 35.

b. Subgroup 2 - Blocking Voltage Life Test
Temperature: $T_C = 125 \pm 6°C$

All of the confirmatory devices were tested for 200 hours, each under the conditions specified, using the method of para. 4.6.2. After exposure to the blocking voltage life test, the reverse current was measured and recorded. The detail data measured is listed in Table 13 and the distribution of the data plotted in Figure 36. All devices passed with margin.

Histogram Data (6)

```
LOWER CELL LIMIT,CELL WIDTH AND NUMBER OF CELLS :.45 .05 25
VERT SCALE:1
CHAR:POST SURGE IR
 CHARACTERISTIC-POST SURGE IR
    AVERAGE- 0.712
    SIGMA--- 0.1106345335
    MAXIMUM- 0.82
    MINIMUM- 0.51
    SAMPLE-- 10

  4+        □
  3+        □
  2+    □ □ □
  1+ □ □□□ □
   +++++++++++++++++++++++++
    0 0 0 0 0 0 1 1 1 1 1 1 1
    . . . . . . . . . . . . .
    4 5 6 7 8 9 0 1 2 3 4 5 6
    5 5 5 5 5 5 5 5 5 5 5 5 5
```

No. of Devices

Limit
15 mA Max.

Fig. 33 Post Surge Reverse Current, I_r , (mA)

```
      HISTOGRAM DATA[;5]

LOWER CELL LIMIT,CELL WIDTH AND NUMBER OF CELLS :1.9 .06 25
VERT SCALE:1
CHAR:TRR
      CHARACTERISTIC-TRR
    AVERAGE- 2.7
    SIGMA--- 0.3527668415
    MAXIMUM- 3.2
    MINIMUM- 2
    SAMPLE-- 10

  2+          □     □ □
  1+ □        □  □  □ □ □  □
   +++++++++++++++++++++++++
    1 2 2 2 2 2 2 2 2 2 3 3 3
    . . . . . . . . . . . . .
    9 0 1 2 3 5 6 7 8 9 1 2 3
      2 4 6 8   2 4 6 8   2 4
```

No. of Devices

Limit
15 μsec. Max.

Fig. 34 Reverse Recovery Time, T_{rr} (μsec)

No. of Devices

```
HISTOGRAM DATA[;7]
LOWER CELL LIMIT,CELL WIDTH AND NUMBER OF CELLS :.20 .05 25
VERT SCALE:1
CHAR:POST BARO IR
 CHARACTERISTIC-POST BARO IR
    AVERAGE- 0.631
    SIGMA--- 0.1700620802
    MAXIMUM- 0.72
    MINIMUM- 0.29
    SAMPLE-- 10

 6+             □
 5+             □
 4+             □
 3+             □
 2+            □□
 1+ □□         □□
  +++++++++++++++++++++++++
    0 0 0 0 0 0 0 0 1 1 1 1 1
    . . . . . . . .   . . . .
    2 3 4 5 6 7 8 9   1 2 3 4
```

Limit
15 mA Max.

Fig. 35 Post Barometric Pressure Reverse Current, I_r (mA)

No. of Devices

```
HISTOGRAM DATA[;8]
LOWER CELL LIMIT,CELL WIDTH AND NUMBER OF CELLS :.04 .05 25
VERT SCALE:1
CHAR:POST BVLT IR
 CHARACTERISTIC-POST BVLT IR
    AVERAGE- 0.654
    SIGMA--- 0.1024369725
    MAXIMUM- 0.72
    MINIMUM- 0.46
    SAMPLE-- 10

 8+                 □
 7+                 □
 6+                 □
 5+                 □
 4+                 □
 3+                 □
 2+           □     □
 1+           □     □
  +++++++++++++++++++++++++
    0 0 0 0 0 0 0 0 0 0 1 1 1
    . . . . . . . . . . . . .
    0 1 2 3 4 5 6 7 8 9 0 1 2
    4 4 4 4 4 4 4 4 4 4 4 4 4
```

Limit
15 mA Max.

Fig. 36 Post Blocking Voltage Reverse Current, I_r (mA)

TABLE 13

Post Environmental Data

Date 8/29/79

Tester P. Bransby

	Post Blocking Voltage L.T.	Post Thermal Shock Test	Post Thermal Shock and Moisture Test	Post Salt Spray Test	Post Shock and Vibration Test	Post Thermal Fatigue L.T.	Post Thermal Fatigue Thermal Resistance Test	Final Envir. Thermal Resistance Test
Method	Par. 4.6.2	1051.1	1021.1 1051.1	1041.1	2016.2, 2056	Par. 4.6.3	Par. 4.6.1	Par. 4.6.1
Symbol	i_r	i_r	i_r	i_r	i_r	i_r	$R_{\theta jc}$	$R_{\theta jc}$
Units	mA	mA	mA	mA	mA	mA	°C/W	°C/W
Ser. No.								
J149	0.70	0.69	--	--	--	0.70	0.13	--
J150	0.70	0.69	--	--	--	0.70	0.10	--
J151	0.70	0.61	--	--	0.72	0.70	0.12	0.16
J156	0.70	0.60	--	--	0.67	0.57	0.14	0.14
J157	0.72	0.50	--	--	0.74	0.70	0.098	0.10
J160	0.70	0.50	--	--	--	0.70	0.10	--
J162	0.70	0.60	--	--	--	0.78	0.09	--
J163	0.70	0.50	--	--	--	0.72	0.15	--
II2	0.46	--	0.41	0.41	0.46	0.56	0.2	--
II3	0.46	--	0.41	0.41	0.46	0.56	0.19	--
Spec.	15 (Max.)	15 (Max.)	15 (Max.)	15 (Max.)	15 (Max.)	15 (Max.)	0.2 (Max.)	0.2 (Max.)

The test plan required that only three devices be tested for this parameter. Since four different types of devices made up the samples (see Sec. B) it was decided that all ten devices should be tested for this parameter for a complete evaluation.

c. Subgroup 3 - Thermal Shock, Moisture Resistance and Salt Atmosphere Tests

All the confirmatory devices were tested for Thermal Shock using test method 1051.1 and the conditions stated in the specification. After five cycles, the rectifiers were removed from the environmental chamber and two were submitted to the Moisture Resistance test, method 1021.1.

Reverse current measurements per Subgroup 2 of Table 1 of the specifications were taken as a check at this point to determine if the devices had survived the Thermal Shock and moisture Resistance tests. All the units passed. Detail data is listed in Table 13 and the distributions plotted in Figures 37 and 38.

The two devices (II2, II3) which had been subjected to the Moisture Test were subjected to the Salt Atmosphere test method 1041.1 for 24 hours. After the test, the salt was washed off of the devices which were then examined. The markings were legible and there was no evidence of flaking, pitting of the finish, or corrosion that would interfere with the application of the devices.

Reverse current tests per Subgroup 2 of Table 1 of the specification were performed, the detail data are listed in Table 13 and the distribution is plotted in Figure 39. All devices passed with margin.

Histogram Data (9)

```
LOWER CELL LIMIT,CELL WIDTH AND NUMBER OF CELLS :.40 .02 25
VERT SCALE:1
CHAR:POST THER SH
 CHARACTERISTIC-POST THER SH
   AVERAGE- 0.58625
   SIGMA--- 0.0799888851
   MAXIMUM- 0.69
   MINIMUM- 0.5
   SAMPLE-- 8

  3+      □    □
  2+      □    □   □
  1+      □    □   □
   +++++++++++++++++++++++++
    0 0 0 0 0 0 0 0 0 0 0 0 0
    . . . . . . . . . . . . .
    4 4 4 5 5 6 6 6 7 7 8 8 8
      4 8 2 6   4 8 2 6   4 8
```

No. of Devices

Limit
15 mA Max.

Fig. 37 Post Thermal Shock Reverse Current, I_r (mA)

Histogram Data (10)

```
LOWER CELL LIMIT,CELL WIDTH AND NUMBER OF CELLS :.35 .02 25
VERT SCALE:1
CHAR:TH SH MO
   CHARACTERISTIC TH SH MO
        AVERAGE- 0.41
        SIGMA--- 0
        MAXIMUM- 0.41
        MINIMUM- 0.41
        SAMPLE-- 2

  2+    □
  1+    □
   +++++++++++++++++++++++++
    0 0 0 0 0 0 0 0 0 0 0 0 0
    . . . . . . . . . . . . .
    3 3 4 4 5 5 5 6 6 7 7 7 8
    5 9 3 7 1 5 9 3 7 1 5 9 3
```

No. of Devices

Limit
15 mA Max.

Fig. 38 Post Thermal Shock and Moisture Reverse Current, I_r (mA)

d. Subgroup 4 - Thermal Fatigue TEst

All of the confirmatory samples were tested for reliability under the specified Thermal Fatigue Test Conditions and Spec. paragraph 4.5.3. The "on" and "off" times were two minutes each. The air flow across the devices was adjusted so that when the devices were conducting, the case or heat-pipe temperature was 90 ± 10°C max. and 30 ± 10°C min. The devices were subjected toa minimum of 200 "on-off" cycles. Ten measurements per Subgroup 2 of Table 1 were made. Detail data are listed in Table 13 and distribution is plotted in Figure 40.

Since the sample consisted of four different constructions, an additional post thermal fatigue parameter was measured, Thermal Impedance. These data are listed in Table 13 and the distribution is plotted in Figure 41.

All devices passed. The ion-implanted devices came closest to the specification limit of 0.2°C/W. Because of this high thermal impedance and other considerations ion-implanted devices will not be used in the pilot run of this MM&T contract.

e. Subgroup 5 - Shock & Vibration Tests

Five of the confirmatory samples were shock tested in RCA's Environmental Laboratory, Lancaster, PA using the specified conditions and test method 2016.2.

Following the shock tests, all devices were subjected to a vibration test of variable frequency described in the Specification and Test Method 2056. After the shock and vibration tests, the reverse current measurements at 800 volts and the thermal resistance measurements of Subgroups 2 and 3 of Table 1 were repeated successfully to verify the integrity of the devices. Detail data are listed in Table 13 and the distributions are plotted in Figures 42 and 43.

Histogram Data (11)

```
LOWER CELL LIMIT,CELL WIDTH AND NUMBER OF CELLS :.35 .01 25
VERT SCALE:1
CHAR:POST SALT SP
 CHARACTERISTIC-POST SALT SP
        AVERAGE- 0.41
        SIGMA--- 0
        MAXIMUM- 0.41
        MINIMUM- 0.41
        SAMPLE-- 2

  2+       □
  1+       □
   +++++++++++++++++++++++++
    0 0 0 0 0 0 0 0 0 0 0 0 0
    . . . . . . . . . . . . .
    3 3 3 4 4 4 4 4 5 5 5 5 5
    5 7 9 1 3 5 7 9 1 3 5 7 9
```

No. of Devices

Limit
15 mA Max.

Fig. 39 Post Salt Spray Reverse Current, I_r, (mA)

```
HISTOGRAM DATA[;13]
LOWER CELL LIMIT,CELL WIDTH AND NUMBER OF CELLS :.45 .05 25
VERT SCALE:1
CHAR:POST TH FRT
  CHARACTERISTIC-POST TH FRT
    AVERAGE- 0.669
    SIGMA--- 0.0769487564
    MAXIMUM- 0.78
    MINIMUM- 0.56
    SAMPLE-- 10

  6+     □
  5+     □
  4+     □
  3+  □  □
  2+  □  □
  1+  □  □□
   +++++++++++++++++++++++++
    0 0 0 0 0 0 1 1 1 1 1 1 1
    . . . . . . . . . . . . .
    4 5 6 7 8 9 0 1 2 3 4 5 6
    5 5 5 5 5 5 5 5 5 5 5 5 5
```

No. of Devices

Limit
15 mA Max.

Fig. 40 Post Thermal Fatigue Reverse Current, I_r (mA)

```
HISTOGRAM DATA[;14]

LOWER CELL LIMIT,CELL WIDTH AND NUMBER OF CELLS :.07 .03 25
VERT SCALE:1
CHAR:POST ENVR RθJC
CHARACTERISTIC-POST ENVR RθJC
   AVERAGE- 0.1318
   SIGMA--- 0.03871778231
   MAXIMUM- 0.2
   MINIMUM- 0.09
   SAMPLE-- 10

 4+ □
 3+ □□
 2+ □□ □       Limit
 1+ □□□□     0.2° C/W Max.
 +++++++++++++++++++++++++
   0 0 0 0 0 0 0 0 0 0 0 0 0
   . . . . . . . . . . . . .
   0 1 1 2 3 3 4 4 5 6 6 7 7
   7 3 9 5 1 7 3 9 5 1 7 3 9
```

No. of Devices

Fig. 41 Post Thermal Fatigue Thermal Impedance (°C/W)

```
Histogram Data (12)

LOWER CELL LIMIT,CELL WIDTH AND NUMBER OF CELLS :.40 .05 25
VERT SCALE:1
CHAR:SH VIR
    CHARACTERISTIC-SH VIR
    AVERAGE- 0.61
    SIGMA--- 0.1392838828
    MAXIMUM- 0.74
    MINIMUM- 0.46                    Limit
    SAMPLE-- 5                     15 mA Max.

 2+ □    □
 1+ □   □□
 +++++++++++++++++++++++++++
   0 0 0 0 0 0 1 1 1 1 1 1 1
   . . . . . .   . . . . . .
   4 5 6 7 8 9   1 2 3 4 5 6
```

No. of Devices

Fig. 42 Post Shock and Vibration Reverse Current, I_r (mA)

Histogram Data (15)

```
LOWER CELL LIMIT,CELL WIDTH AND NUMBER OF CELLS :.08 .02 25
VERT SCALE:1
CHAR:FIN ENVR RθJC
 CHARACTERISTIC-FIN ENVR RθJC
   AVERAGE- 0.1333333333
   SIGMA--- 0.03055050463
   MAXIMUM- 0.16
   MINIMUM- 0.1
   SAMPLE-- 3                   Limit
              |                0.2°C/W Max.
  1+ □ □□     |
   +++++++++++++++++++++++++
    0 0 0 0 0 0 0 0 0 0 0 0 0
    . . . . . . . . . . . . .
    0 1 1 2 2 2 3 3 4 4 4 5 5
    8 2 6   4 8 2 6   4 8 2 6
```

No. of Devices

Fig. 43 Post Shock and Vibration Thermal Resistance, $R_{\theta JC}$ (°C/W

```
     HISTOGRAM DATA[;16]

LOWER CELL LIMIT,CELL WIDTH AND NUMBER OF CELLS :3.5 .5 25
VERT SCALE:1
CHAR:DIM A
     CHARACTERISTIC-DIM A
   AVERAGE- 4.744
   SIGMA--- 0.01433720878
   MAXIMUM- 4.761
   MINIMUM- 4.718
   SAMPLE-- 10

 10+  □
  9+  □
  8+  □
  7+  □
  6+  □
  5+  □
  4+  □
  3+  □
  2+  □
  1+  □
   +++++++++++++++++++++++++
    3 4 5 6 7 8 9 1 1 1 1 1 1
    . . . . . . . 0 1 2 3 4 5
    5 5 5 5 5 5 5 . . . . . .
                  5 5 5 5 5 5
```

No. of Devices

Fig. 44 Statistical Distribution of Dimension A

The Acceptance Test Procedure required that only two devices be subjected to the Shock and Vibration Tests. Since four different constructions were represented in the sample, RCA subjected a sample of each to the environmental test as follows:

No. of Devices	Construction
1	Webless Wicked
1	Convoluted Tungsten Button
1	Nonconvoluted Tungsten Button
2	Ion-Implanted

Again all devices passed. The Thermal Resistance data listed for II2 and II3 were measured after the Shock and Vibration Tests.

4. General Data

Table 14 lists a statistical analysis of all the data measured during this confirmatory test. Table 15 lists the key for identifying the individual characteristics. Figures 44, 45, 46, 47 and 48 show the distribution of the dimensions of the samples.

5. Engineering Evaluations

a. Low Temperature Thermal Shock

In addition to the required tests discussed, two nonconvoluted devices with tungsten buttons were subjected to two complete thermal shock test using method 1051.1 and a low temperature of $-55^{\circ}C$ instead of the specified $-25^{\circ}C$. This action results in doubling the number of nonconvoluted devices tested, doubling the number of cycles to 10 instead of 5, and doubling the stress to $-55^{\circ}C$ instead of $-25^{\circ}C$. Both devices passed with flying colors.

S/N	Reverse Current (I_r) mA	Thermal Resistance ($R_{\Theta JC}$) $^{\circ}C/W$	
J155	0.82	0.1	initial data
	0.1	0.15	after test
J158	0.87	0.09	initial data
	0.1	0.12	after test

Table 14

Statistical Analysis of Confirmatory Data

PRODUCT------CONFIMATORY SILICON TRANSCALENT RECTIFIER DATA						
CHARACTERISTIC	AVG	SIGMA	MAX	MIN	CHI-SQ	N
1	.822	.125	.920	.610	21.20	10
2	2.857	1.732	6.180	1.440	12.85	10
3	.114	.047	.200	.070	18.89	10
4	.988	.025	1.000	.920	19.69	10
5	2.700	.353	3.200	2.000	4.71	10
6	.712	.111	.820	.510	8.26	10
7	.631	.170	.720	.290	23.41	10
8	.654	.102	.720	.460	26.26	10
9	.586	.080	.690	.500	16.37	8
10	.410		.410	.410	2.00	2
11	.410		.410	.410	2.00	2
12	.610	.139	.740	.460	9.71	5
13	.669	.077	.780	.560	14.74	10
14	.132	.039	.200	.090	11.12	10
15	.133	.031	.160	.100	4.30	3
16	4.744	.014	4.761	4.718	8.38	10
17	3.463	.009	3.476	3.447	2.95	10
18	.636	.008	.650	.624	3.82	10
19	1.804	.012	1.834	1.790	12.40	10
20	2.102	.002	2.106	2.100	15.21	10

TUESDAY, OCTOBER 9,1979

Table 15

Key to Statistical Analysis of Table 14

Characteristic #	Definition
1	Reverse Current (I_r) at +25°C
2	Reverse Current (I_r) at +125°C
3	Thermal Impedance $R_{\theta JC}$
4	Forward Voltage (V_{FM})
5	Reverse Recovery Time (T_{rr})
6	Post Surge Test, Reverse Current (I_r)
7	Post Barometric Test, Reverse Current (I_r)
8	Post Blocking Voltage Life Test, Reverse Current (I_r)
9	Post Thermal Shock Test, Reverse Current (I_r)
10	Post Thermal Shock & Moisture Test, Reverse Current (I_r)
11	Post Salt Spray Test. Reverse Current (I_r)
12	Post Shock & Vibration Test, Reverse Current (I_r)
13	Post Thermal Fatigue Test, Reverse Current (I_r)
14	Post Environmental Test, Thermal Resistance ($R_{\theta JC}$)
15	Final Environmental Test, Thermal Resistance ($R_{\theta JC}$)
16	Dimension A
17	Dimension B
18	Dimension C
19	Dimension D
20	Dimension F

```
      HISTOGRAM DATA[;17]
LOWER CELL LIMIT,CELL WIDTH AND NUMBER OF CELLS :1.5 .5 25
VERT SCALE:1
CHAR:DIM B
     CHARACTERISTIC-DIM B
   AVERAGE- 3.4633
   SIGMA--- 0.008844960901
   MAXIMUM- 3.476
   MINIMUM- 3.447
   SAMPLE-- 10

  10+    □
   9+    □
   8+    □
   7+    □
   6+    □
   5+    □
   4+    □
   3+    □
   2+    □
   1+    □
   +++++++++++++++++++++++++++
    1 2 3 4 5 6 7 8 9 1 1 1 1
    . . . . . . . . . 0 1 2 3
    5 5 5 5 5 5 5 5 5 . . . .
                      5 5 5 5
```

No. of Devices

Fig. 45 Statistical Distribution of Dimension B

```
   HISTOGRAM DATA[;18]
LOWER CELL LIMIT,CELL WIDTH AND NUMBER OF CELLS :.45 .05 25
VERT SCALE:1
CHAR:DIM C
     CHARACTERISTIC-DIM C
   AVERAGE- 0.6363
   SIGMA--- 0.008219894565
   MAXIMUM- 0.65
   MINIMUM- 0.624
   SAMPLE-- 10

   9+    □
   8+    □
   7+    □
   6+    □
   5+    □
   4+    □
   3+    □
   2+    □
   1+    □□
   +++++++++++++++++++++++++++
    0 0 0 0 0 0 1 1 1 1 1 1 1
    . . . . . . . . . . . . .
    4 5 6 7 8 9 0 1 2 3 4 5 6
    5 5 5 5 5 5 5 5 5 5 5 5 5
```

No. of Devices

Fig. 46 Statistical Distribution of Dimension C

```
     HISTOGRAM DATA[;19]

LOWER CELL LIMIT,CELL WIDTH AND NUMBER OF CELLS :.5 .3 25
VERT SCALE:1
CHAR:DIM D
     CHARACTERISTIC-DIM D
   AVERAGE- 1.8042
   SIGMA--- 0.01198888374
   MAXIMUM- 1.834
   MINIMUM- 1.79
   SAMPLE-- 10

  8+      □
  7+      □
  6+      □
  5+      □
  4+      □
  3+      □
  2+     □□
  1+     □□
   +++++++++++++++++++++++++
    0 1 1 2 2 3 4 4 5 5 6 7 7
    . . . . . . . . . . . . .
    5 1 7 3 9 5 1 7 3 9 5 1 7
```

No. of Devices

Fig. 47 Statistical Distribution of Dimension D

```
     HISTOGRAM DATA[;20]

LOWER CELL LIMIT,CELL WIDTH AND NUMBER OF CELLS :1.5 .1 25
VERT SCALE:1
CHAR:DIM F
     CHARACTERISTIC-DIM F
   AVERAGE- 2.1015
   SIGMA--- 0.002068278941
   MAXIMUM- 2.106
   MINIMUM- 2.1
   SAMPLE-- 10

 10+       □
  9+       □
  8+       □
  7+       □
  6+       □
  5+       □
  4+       □
  3+       □
  2+       □
  1+       □
   +++++++++++++++++++++++++
    1 1 1 2 2 2 2 2 3 3 3 3 3
    . . . . . . . . . . . . .
    5 7 9 1 3 5 7 9 1 3 5 7 9
```

No. of Devices

Fig. 48 Statistical Distribution of Dimension F

b. High Temperature Life Test

Transcalent rectifier serial number F147 was tested for 979.8 hours at a case temperature of $+175^{\circ}C$. The test was the standard reverse blocking voltage life test, except for the case temperature which was maintained at $+175^{\circ}C$ instead of $+125^{\circ}C$. See section V-E for a detail description of the life test equipment.

At the end of 979.8 hours the device was still capable of holding off 800 volts reverse voltage. At the end of the test, the unit was tested for thermal resistance ($R_{\theta JC}$) and dissected to determine if any creeping of the heat-pipes had occurred.

Observations:

1. $R_{\theta JC}$ increased from $0.12^{\circ}C$/Watt at zero hours to $0.23^{\circ}C$/Watt at 979.8 hours.

2. The wafer solder integrity was excellent.

3. No bulging in the convolution was noted.

4. All internal dimensions remained the same.

Conclusion:

The unit's physical integrity was not degraded by long term operation at a case temperature of $+175^{\circ}C$.

V. Test Equipment

Refer to the First through Sixth Monthly Reports for this contract for additional information concerning test apparatus. The electrical and environmental test equipment survey is listed in Table 16.

A. Surge Current Test Set

The surge current test is a survival test which demonstrates that a rectifier is capable of conducting unusually large amounts of current without

TABLE 16

ELECTRICAL AND ENVIRONMENTAL TEST EQUIPMENT

Method	Test Description	Status of Facility
2066	Physical Dimensions	Precision Vernier Calipers and "go-no-go" gauge available.
4016.2	Reverse Current	Facilities available for A.C. Method. Temperature Controlled Oven available.
Par. 4.6.1	Thermal Resistance	Engineering Test Facility available.
4011.3	Forward Voltage	Power Supply and Monitoring available.
4066.2	Surge Current	Surge Fwd. Current and Rev. Voltage Supplies are available.
4031	Reverse Recovery Time	JEDEC Test Circuit developed and test results correlate with RCA, Somerville, NJ, test data. Test equipment is operational.
1001.1	Barometric Pressure (reduced)	Vacuum Chamber and V_r Supply available. Supply modified for half-wave operation.
Par. 4.6.2	Blocking-Voltage Life Test	Oven and Supply are available. Supply modified for half-wave operation.
1051.1	Thermal Shock (Temperature Cycling)	Test facility available at RCA, Lancaster, Environmental Test Laboratory.
1021.1	Moisture Resistance	Ditto
2016.2	Shock	Ditto
2056	Vibration, Variable Frequencies	Ditto

TABLE 16 (Cont.)

ELECTRICAL AND ENVIRONMENTAL TEST EQUIPMENT

Method	Test Description	Status of Facility
1041.1	Salt Atmosphere (corrosion)	Test facility available at RCA, Lancaster, Environmental Test Laboratory.
Par. 4.6.3	Thermal Fatigue Test	Power Supply and Controller are available.

DRT 9/22/78
MFD 1/10/79
MFD 9/25/79

being destroyed. In the surge test, there are four distinct, sequential circuit functions;

Application of 250 amperes average (400 amperes RMS) of "on" state heating current to bring the rectifier junction to its normal operating temperature,

Application of one 60 Hz, positive, 1/2 cycle high current surge to the DUT,

Application of one 60 Hz, negative, 1/2 cycle reverse high voltage pulse to the DUT.

The above test sequence of operations is repeated at one minute intervals for 10 total surges.

The repetitive surge current test set is shown in Figure 49. The circuit block diagram is illustrated in Figure 50. Three power supplies are also involved in this test of DUT's ability to withstand overloads. Sequencing on the exact half or full 60 Hz cycle is designed into the equipment. High voltage interlocks are used for safety of the operating personnel.

An a.c. heating current supply heats the DUT to its normal operating temperature before a second supply applies a single, half cycle forward current surge to the DUT. On the subsequent half cycle, an 800 volts peak reverse a.c. voltage is applied to test whether the device has retained its blocking capability following the surge. This surge sequence is repeated ten times at one minute intervals. All parameters are recorded temporarily on a storage oscilloscope for accurate readings.

Other test conditions, such as, higher peak surges, lower reverse voltages and different time intervals can be set up, if desired. Forced air cooling is utilized.

B. Forward On-State Voltage Test Set

In the forward on-state voltage test the peak forward voltage drop is measured while the rectifier is conducting its rated current. At the same time the operation of the heat-pipes is confirmed.

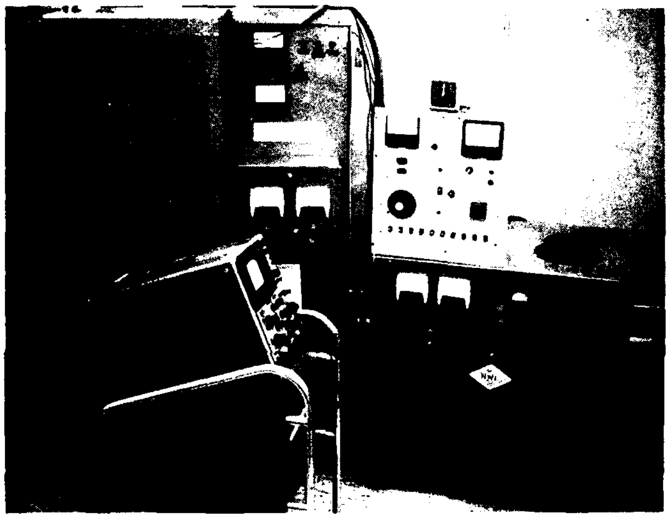
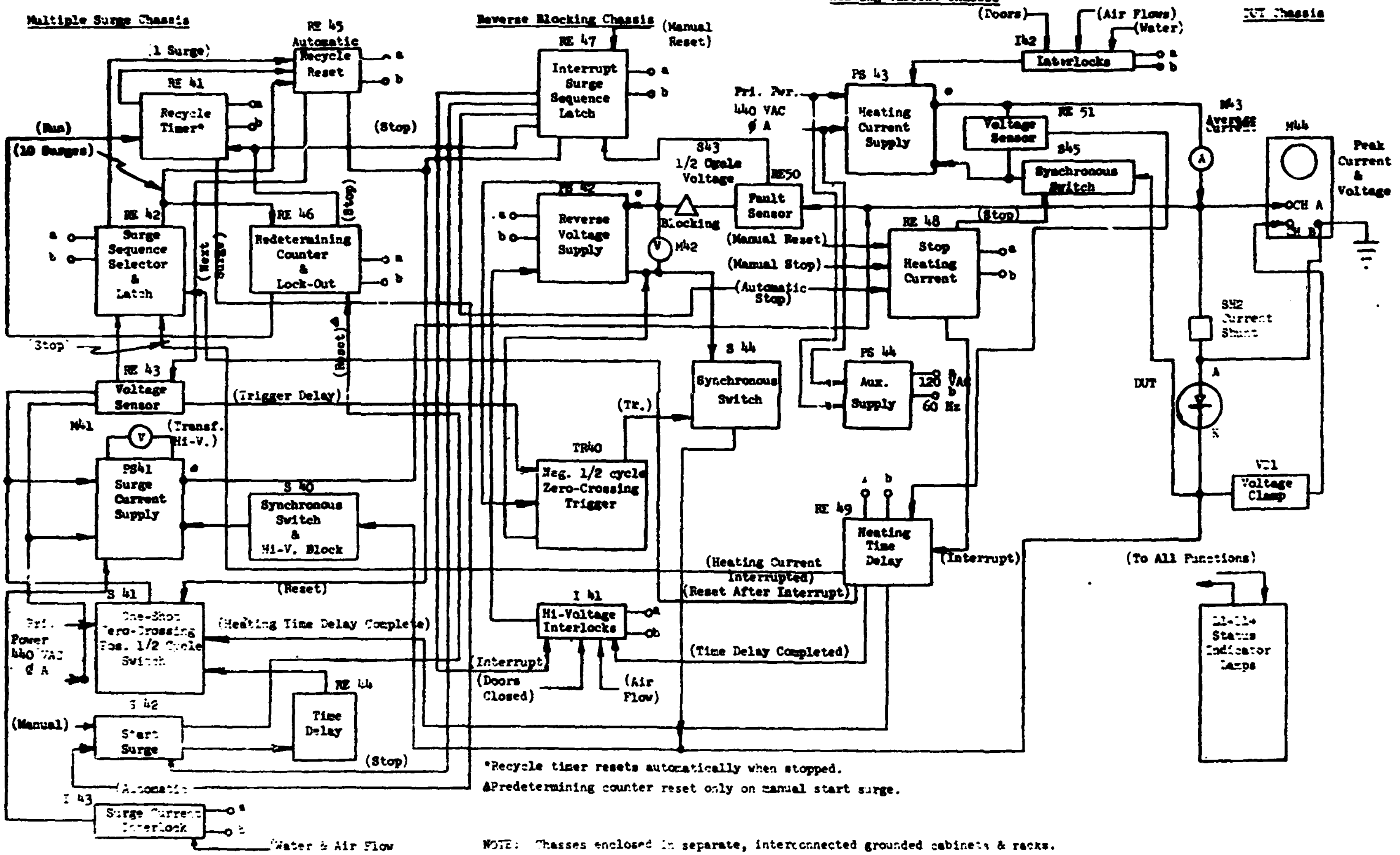


Figure 49 Repetitive Surge Current Test Set. The DUT was mounted inside the interlocked door on the left in the photograph

Semi-Automatic Multiple Surge Current Test Set - Reapplied Rev. Voltage

1/8'77 RFR

Functional Block Diagram



*Recycle timer resets automatically when stopped.

ΔPredetermining counter reset only on manual start surge.

NOTE: Chasses enclosed in separate, interconnected grounded cabinets & racks.

Figure 50

The test set shown in Figure 51 applies the full rated average a.c. current to the DUT. The cooling air flow is adjusted to achieve the required 100°C on the case of the heat-pipe of the DUT before the peak forward voltage is read on the oscilloscope. A functional block diagram of the circuit is shown in Figure 52.

During this test the temperature is measured at several points along the heat-pipes. In this way, the heat-pipes' thermal balance and isothermal characteristics can be verified. A poorly functioning heat-pipe is not isothermal. Properly functioning heat-pipes are important not only for the reliability of the DUT, but also because the on-state voltage is a function of the junction temperature.

C. Thermal Fatigue Test Set

Rectifiers are temperature cycled by operating them in a circuit in which the devices are heated by conducting their full rated current of 250 A average and cooled by blowing room temperature air across the fins on the device. The test is conducted for a minimum of 200 cycles. The test set is shown in Figure 53 along with the functional block diagram of the circuit in Figure 54. The air flow is adjustable to assure that the specified minimum and maximum (Min. $T_C = 30 \pm 10^{\circ}C$, Max. $T_C = 90 \pm 10^{\circ}C$) temperatures are achieved on every cycle. A recorder connected to a thermocouple attached to the rectifier is used to verify not only the temperature range, but also the number of cycles.

D. Blocking Current Test Set

The blocking current test set is used to measure the leakage currents of the reverse blocking junction. The test set along with the functional block diagram of the circuit are shown in Figures 55 and 56, respectively. The reverse blocking (leakage) currents are measured at the full rated a.c. voltage of 800 volts peak. These currents are measured at both room temperature (25°C) and at the maximum rated temperature (125°C) of the Device Under Test (DUT).

The measurement is performed by monitoring the voltage drop across a calibrated resistor in series with the DUT. This enables an oscilloscope to be used to measure the peak current since the oscilloscope is a voltage rather than a current measuring device. Ohm's law converts the reading to the current.

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MANUFACTURING METHODS AND TECHNOLOGY MEASURE FOR FABRICATION OF--ETC(U)
SEP 80 B B ADAMS, M F DEVITO, R E REED   DAAK70-78-C-0120

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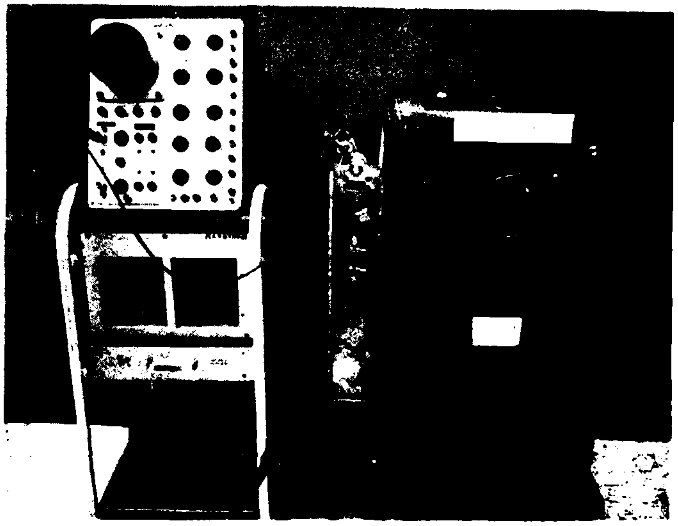


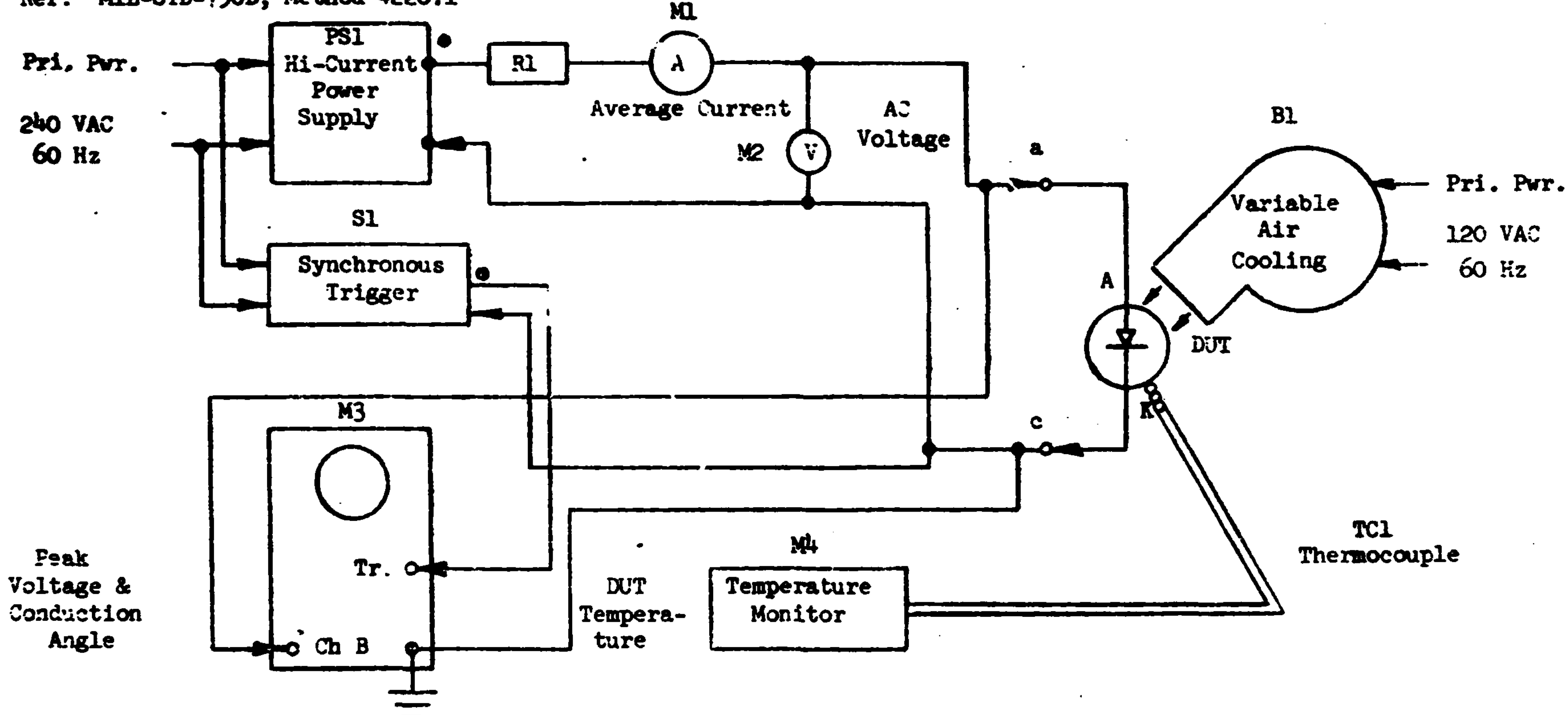
Figure 51 Forward On-State Voltage Test Set. The DUT was mounted at the top of the cooling air duct in the center of the photograph.

1/12/77 RER
1/10/79 MFT

Figure 52 Forward "ON" Voltage Test Set - Portable

Block Diagram

Ref: MIL-STD-750B, Method 4226.1



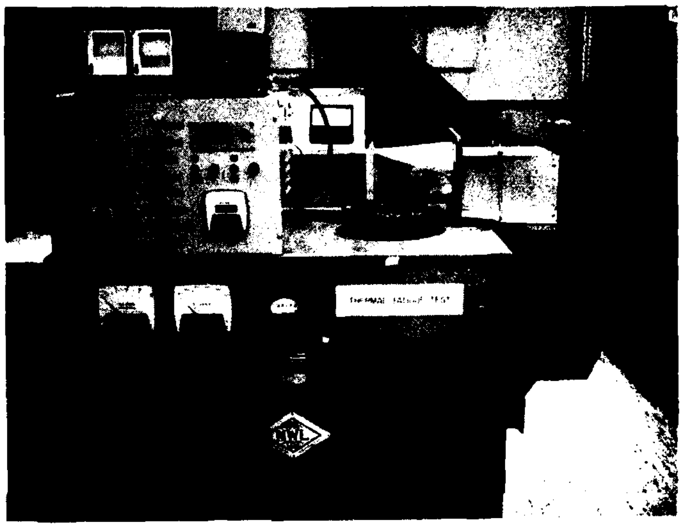


Fig. 53 Thermal Fatigue Test Set. The DUT's are mounted out of view in the end of the air cooling duct at the back of the test set.

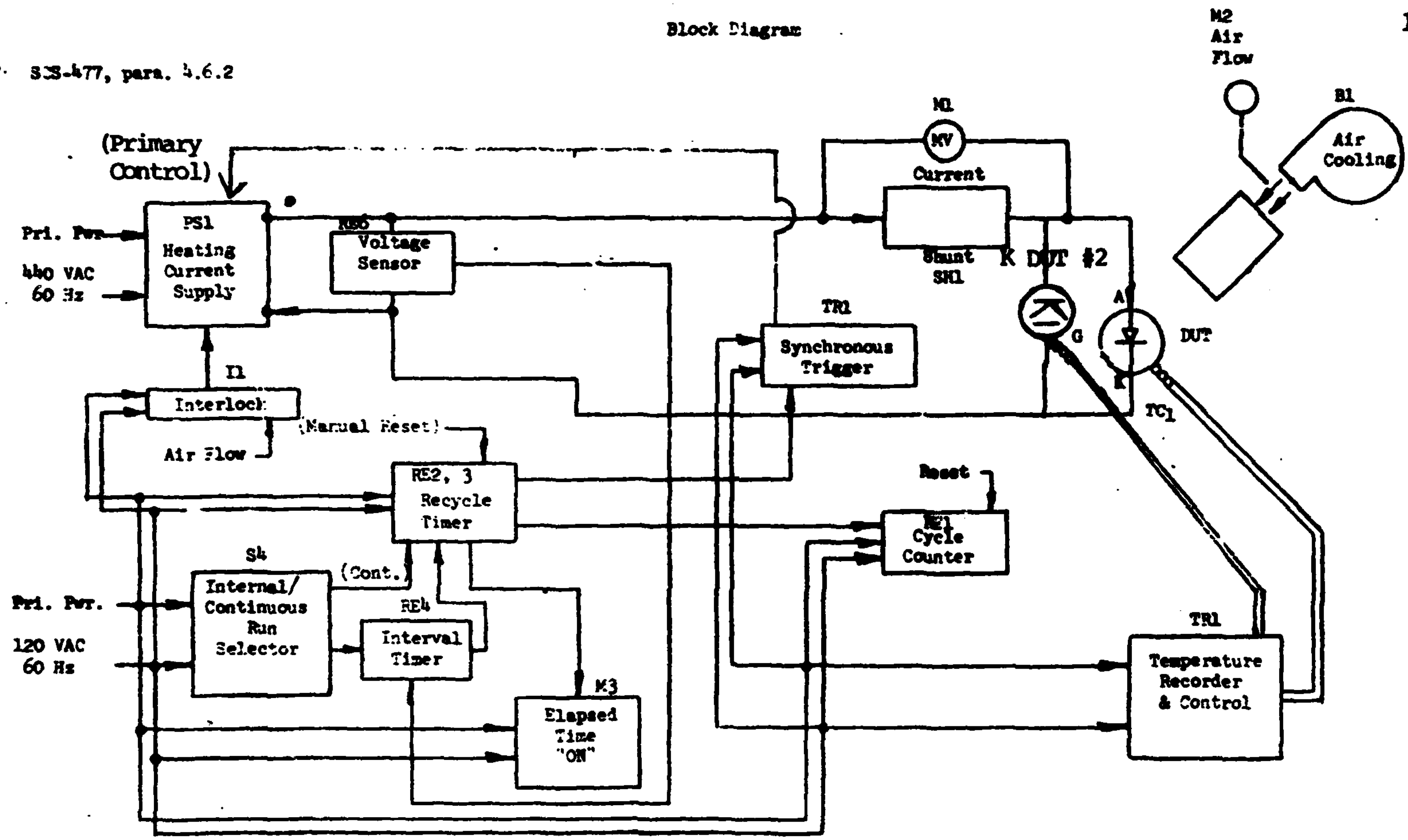
Figure 54 Thermal Fatigue Test Set

Block Diagram

1/13/77 [illegible]

1/10/79 MD

Ref· SCS-477, para. 4.6.2



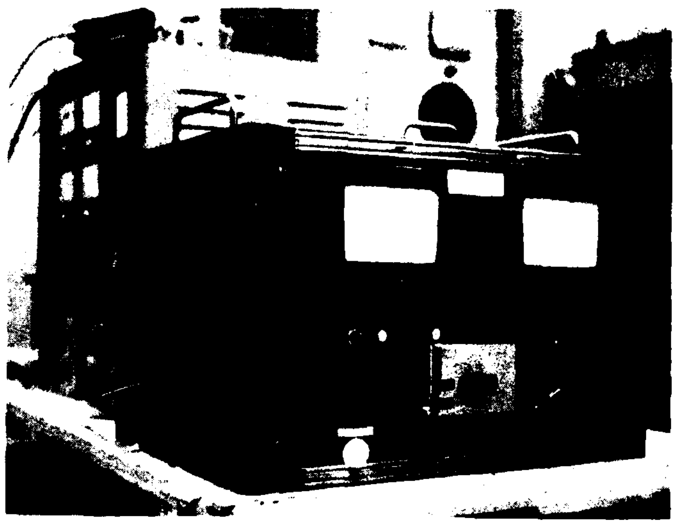


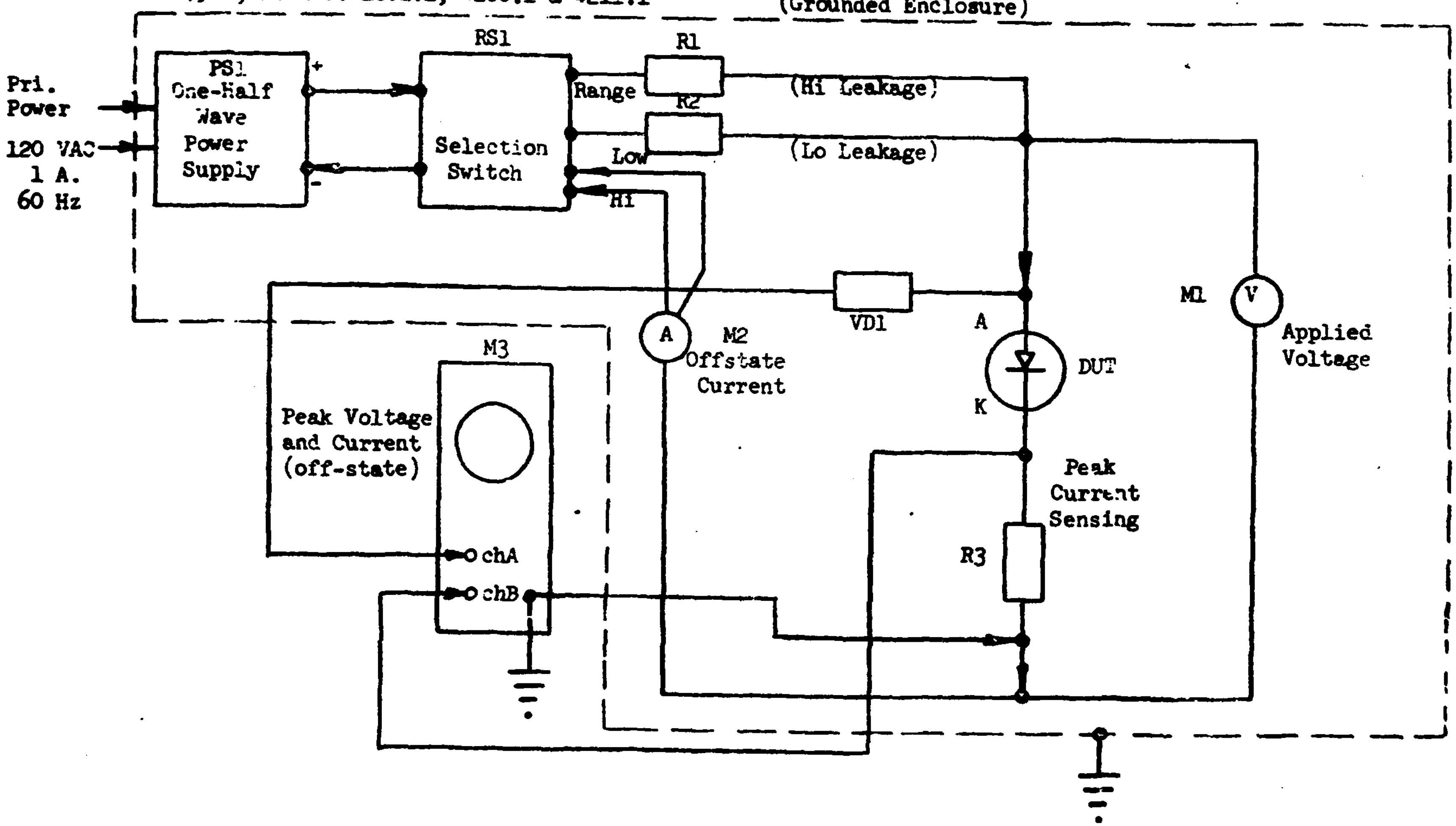
Fig. 55 Blocking Current Test Set. This set was used at room temperature as well as in conjunction with an oven or a vacuum system (not shown) for the high temperature and reduced barometric pressure tests. Reverse blocking currents are measured with this equipment.

Figure 56 Reverse Blocking Current Test Set - A. C. Method

1/7/77
RER

Block Diagram

Ref: MIL-STD 750B, methods 1001.1, 4206.1 & 4211.1



E. Blocking Voltage Life Test

Rectifiers are life tested for 200 hours by subjecting them to reverse blocking voltages of 800 volts while at a temperature of 125°C. A 60 Hz 1/2 wave AC power supply is used for voltage power. The test set is shown in Figure 57 and the functional block diagram is shown in Figure 58.

Metering within the test set provides the temperature of the DUT, elapsed time, voltage and current. A jack is provided for the measurement of the peak voltage with an oscilloscope. Indicator lamps and high voltage fuses are included in the power supply to indicate whether a DUT has failed to block the high voltage during the tests. The test set is designed to test six devices simultaneously.

The power supply is connected through a voltage regulator to the primary power lines of the high temperature oven. In this way, the power and timing are removed from the DUT in the event of a power interruption that would reduce the oven temperature below the test value. An interlocked oven door also removes the high voltage from the DUT when the oven door is opened, thus, protecting the personnel.

This power supply is also used for the Reduced Barometric Pressure test for half wave voltage application to the DUT in the vacuum chamber.

F. Thermal Resistance Test Set

The thermal resistance test set is used to determine the thermal resistance between the junction and the base of the fins on the heat-pipe.

Prior to testing the rectifier, each device is calibrated by recording the forward voltage (V_F) drop at 4.0 A as a function of temperature. At each selected temperature, sufficient time is taken to insure that the junction, the heat-pipes and the oven are all in thermal equilibrium. At 4.0 A, V_F versus temperature is interpreted from measurements of the V_F at temperatures between the selected temperatures.

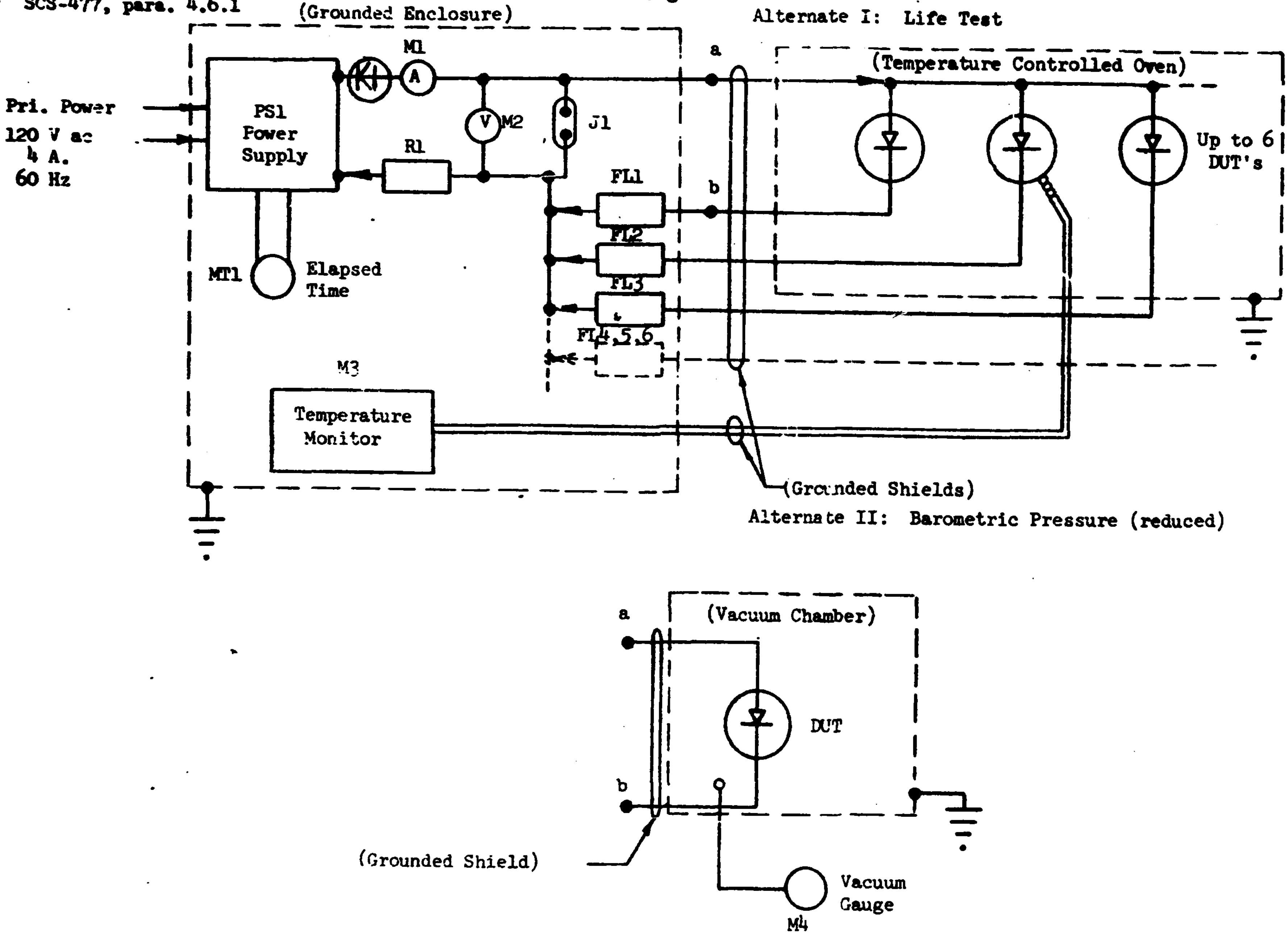
Fig. 57 Blocking Voltage Life Test Set, including the temperature controlled oven. This oven is also used for the other high temperature tests.

Figure 58 Blocking Voltage Life Test/Barometric Pressure Test Set

Block Diagram

1/7/77 RER
1/10/79 MFD

Ref: SCS-477, para. 4.6.1



It is this characteristic of V_F versus temperature at 4.0 A which is employed to determine the junction temperature during the thermal resistance test. The difference between the junction temperature and the case temperature, which is measured with a thermocouple attached to the outside wall of the heat-pipe, divided by heating power is the thermal resistance.

When a rectifier is tested it is heated by passing rated current through the device. This heating current is interrupted every 50.0 ms for about 0.5 ms. During the interruption, the V_F is measured at the calibration current of 4.0 A.

The test set is shown in Figure 59. Figure 60 is a functional block diagram of the circuit.

The thermal resistance of the Transcalent rectifier is a function of dissipation power and ambient temperature.

VI. Specification Control/Configuration Management Program

A. Engineering Specification Control

Specifications for product manufacture, testing and quality control are given in the Engineering Specifications. These specifications (Standardizing Notices) are the official documents used to record and disseminate engineering specifications on electronic components and are developed and maintained by the Engineering Standards activity. These specifications give the details concerning materials, processes, testing procedures, etc., for the products designed and manufactured in SSD-EOD. Quality and Reliability Assurance participates in the establishment of guides listing the mandatory approvers of Engineering Specifications.

B. Engineering Change Proposals (ECPs)

All changes, amendments, delections or deviations from approved Engineering Specifications affecting any standard, custom or development product which has been offered for sale, must be accomplished through the change control system.

The system permits alteration of an accpeted practice after approval by designated qualified reviewers on Change Control Board (CCB) whereby the variation becomes new accepted practice.

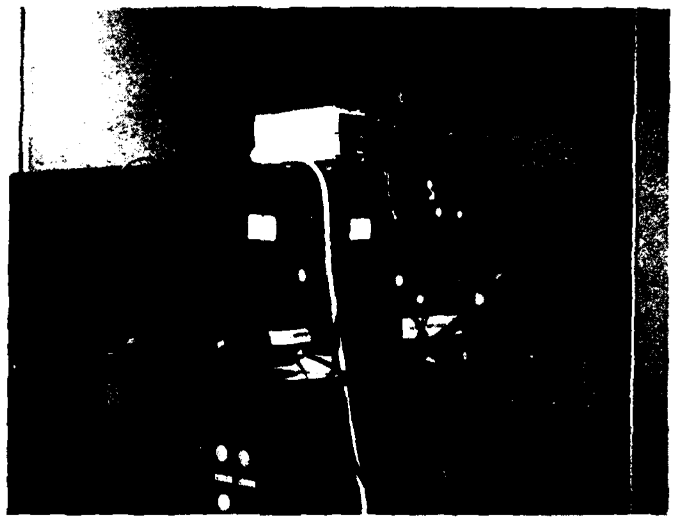


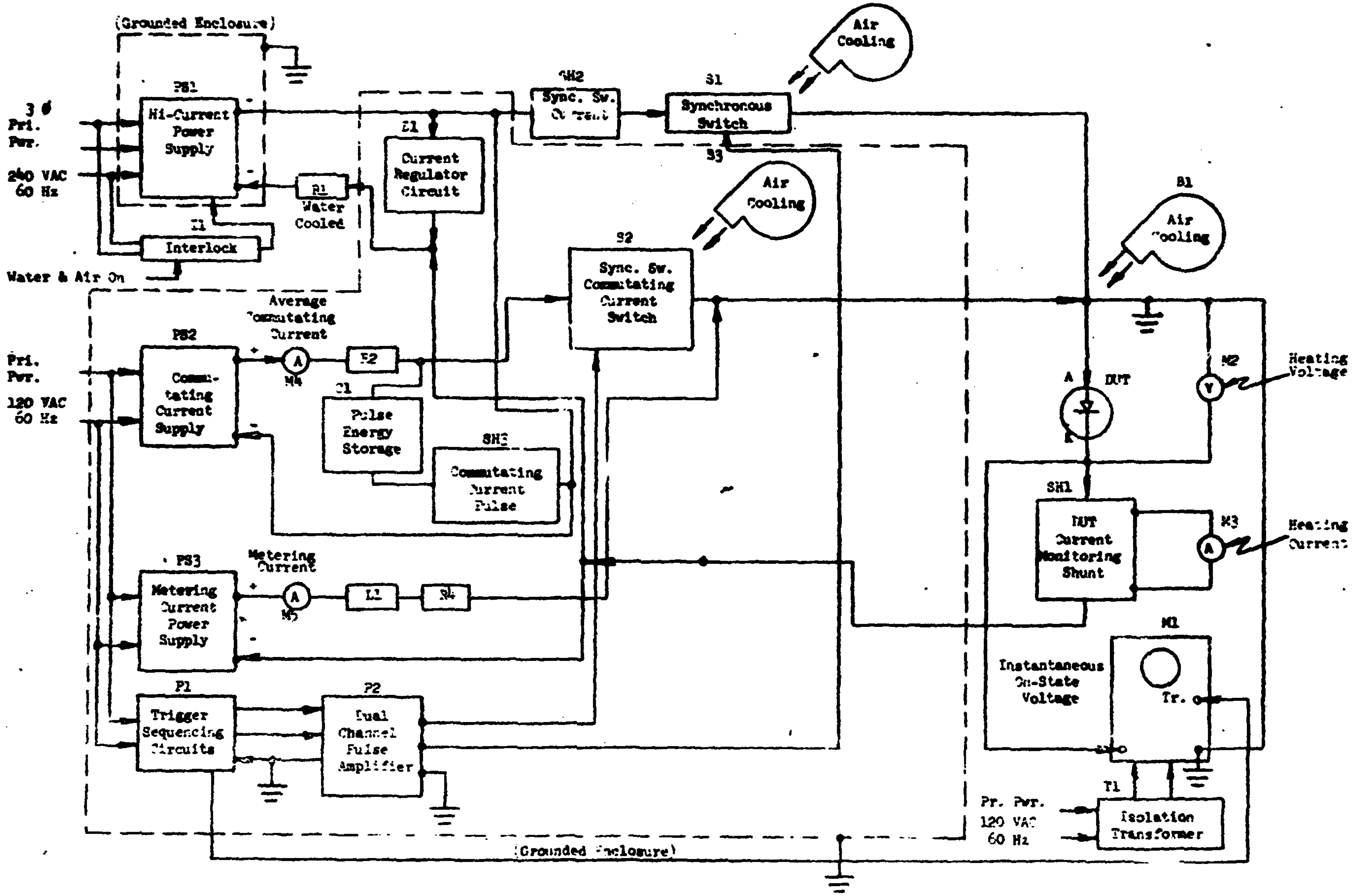
Fig. 59 Thermal Resistance Test Set. The DUT is mounted in the end of the cooling air duct shown in the foreground.

1/10/79 MFD

Figure 60 Thermal Resistance Test Set

Block Diagram

Ref: MIL-STD 750B, Method 3151



C. Configuration Changes

The Engineering Standards Department has established a change control system by which all necessary revisions or additions to specification documents under the jurisdiction of Engineering Standard can be made. The purpose of the system is to provide a uniform method for evaluating the various aspects of an engineering change, to obtain the written approval of all mandatory approvers, to notify all concerned activities of the reply deadline and the effective dates for an engineering change, as well as to provide approvers with a method for approving, revising, rejecting or temporarily withholding approval of an engineering change.

In addition, the secondary purpose of the change system is to notify all cognizant activities of any change affecting the status or content of a specification as well as obtain information, comments, and guidance from the Material Control, Parts Manufacturing and Materials (Purchasing) functions prior to the submittal of the proposed engineering change to the Engineering Standard Department for issue. Note that the engineering change system is not for the purpose of obtaining engineering information. The necessary engineering tests and discussions with all affected activities must be adequately covered prior to the initiation of a Change Notice.

D. Procedures

All in-house activities have ten working days from the issue date to review a change and make any proposed revisions. After fifteen working days, for inter-plant approvals, Engineering Standards will specify the reply deadline and approval (effective dates on the Engineering Change Form) and the change will be effective on that date. Written approval of all mandatory approvers must have been obtained prior to the reply deadline. Mandatory approvers are those persons responsible for effecting product line development and manufacturing as well as quality and reliability assurance of the product. Marketing and Applications Engineering are responsible for securing any necessary customer approvals.

RCA Solid State Fig. 61 **Engineering Change**

Engineering Standards|Electro Optics and Devices|Lancaster, PA 17604 — See ES 1-1-3 Page 60 Series for EC System

Subject	Permanent ✓ / Temporary	Quantity/Date	Dept.	Year	No
Anode Weld Flange	Permanent ✓		L 963	78	106

	Types		
[ ] Developmental	Transcalent Devices	Effective Date ON APPROVAL	Serial/Lot No. N/A
[ ] Pilot	P95000EB2,3,4,5,6	For Engineering Standards Use Only:	Initial Issue / Release
[✓] Custom	P95 00EE4	Issue Date	3-29-78
[ ] Commercial	P95400EB2,3,4,5,6	Reply Deadline Date	——
[ ] Other	Product Line: TRANSCALENT	Approval Date	3-20-78

Present — Engineering Specification & Page No. — **Proposed**

AS specified .... 3025260 .... change .085 min To .060 min.

add Note 5: Dia tol. may vary to +.004 at open end of dia. Add this Note to 1.872 $^{+.000}_{-.005}$ dia.

Purpose

[ ] Initial specification
[ ] Improve product performance (See Supporting Data)
[✓] Clarify or correct specifications
[ ] Contractual or MIL Spec compliance
[ ] Policy or procedure compliance
[ ] Specified material is unobtainable
[ ] Cost reduction
[ ] Product or personnel safety compliance
[ ] Other (See Additional Remarks)

Supporting Data

Change affects finished product performance [✓] No [ ] Yes (If yes attach supporting Test, Env., Life, Rel., etc data)
Affects product or personnel safety [✓] No [ ] Yes (See Additional Remarks)
Proposed change (does, does not) comply with [ ] MIL-Q-9858 ( ) [ ] MIL-I-45208 ( ) [✓] N/A [signature] 3/6/78
Government approval [✓] N/A [ ] Req [ ] Rec'd
EIA approval [✓] N/A [ ] Req [ ] Rec'd
Customer approval [✓] N/A [ ] Req [ ] Rec'd
Estimated cost of change $ ——— (See Additional Remarks)
Disposition of obsolete stock [✓] N/A [ ] See below

Part(s) or Material(s):

Status	Qty.	Value	Use	Scrap
In Process				
In Invent.				
On Order				

Additional Remarks

The above change describes the parts as received from Carlow. It will not effect form fit or function.

Note To Originator
If proposed change affects any of the following, authorized signatures must be obtained before furnishing EC to Engineering Standards.

		Date
Change affects Parts Mfg.	N/A	
Change affects Purchasing	[signature]	3/4/75
Change affects stock inventories	N/A	

T. Dell 3/13

Originator Ben Adams	Standards Rep. [signature]	Endorser [signature]
Date 2/28/78 Tel. No. 2872	Date 3-20-78 Tel. No. 2027	Date 3/2/78 Tel. No. 2485

TI 305 12/75

MAR 17 REC'D

RCA Electro Optics and Devices

Engineering Standards | Lancaster, PA

Fig. 62

ENGINEERING CHANGE PROPOSAL
APPROVAL GUIDE - POWER PRODUCT SUPER.
DATE 10/23/78

This guide lists the official endorsers and approvers for Engineering Change Proposals.

✓ MANDATORY APPROVERS - WRITTEN APPROVAL REQUIRED (Ref: ES 1-1-3)
X OTHER APPROVERS - WRITTEN APPROVAL NOT REQUIRED
Δ INFORMATION ONLY - APPROVAL NOT REQUIRED

ECL

	ACTIVITY	DIST.	APPROVERS		ACTIVITY	DIST	APPROVERS
	POWER TUBE OPERATION		CW BIZAL		ANALYTICAL LAB	1	DF HAKALA
✓	Power Prod. Eng.	3	JG Kindbom				
					PROC. & MATL. DEV.	1	JA ZOLLMAN
	POWER ENGINEERING		WS LYNCH		Adv. Sales Promo & Publ.	1	JF Chattin
	Design	2	CR Carter				
	Appl. & Module	1	CE Doner		O&R Services	1	HL Stewart
	M&P Lab/Transcalent	1	RE Reed				
	Coax Eng. Y1143	1	BB Adams		Warehouse (Lanc.)	1	LH Waltman
	Coax Eng 4668, 4655	1	JA Eshleman				
	Coax Eng., Mfg.	1	JG Kindbom		Color Eng. Stds.	1	GJ McCauley
	Coax Mfg(4655,Y1143)	1	P Harvest				
					Prod. Safety	1	JA Molzahn
	Q&RS ENG.	1	GJ BUCHKO				
	Q&RS ENG. (Transc.)	1	CA MANNON		Safety (Pers.)	1	CH Miller
	MATERIALS		RC PONTZ	Δ	Data Control	1	DC Leayman
	Matl. Handling	2	AA May				
	Matl: Purch. Cont.			Δ	Industrial Eng.	1	GS Diamantoni
	Raw Matls., Pkg. Matls., Chemicals	1	JH Hipp	Δ	Standard Cost	1	EB Tabbutt
	E-O Syst & Equip.	2	RA Brandt				
					Inter. Lic. Serv.	1	AG Krause
	Q&RA FINISH PROD.		JJ CARROLL				
	Fin Prod Test/Eval.	2	HA Kotler	Δ	Patent - Power & EO	1	RM Roderick
	Env. Eng. & Test	1	JB Grosh				
				Δ	Iron Mountain	1	
	TUBE PARTS MFG.	5	RL SPALDING				
				Δ	Originator	1	
	PWR TUBE OPER. CONT.	1	JD SCHMITT				
	PWR TUBE MKT.	1	RM BOWES				

Fig. 63

RCA Electro Optics and Devices

Engineering Standards | Lancaster, PA

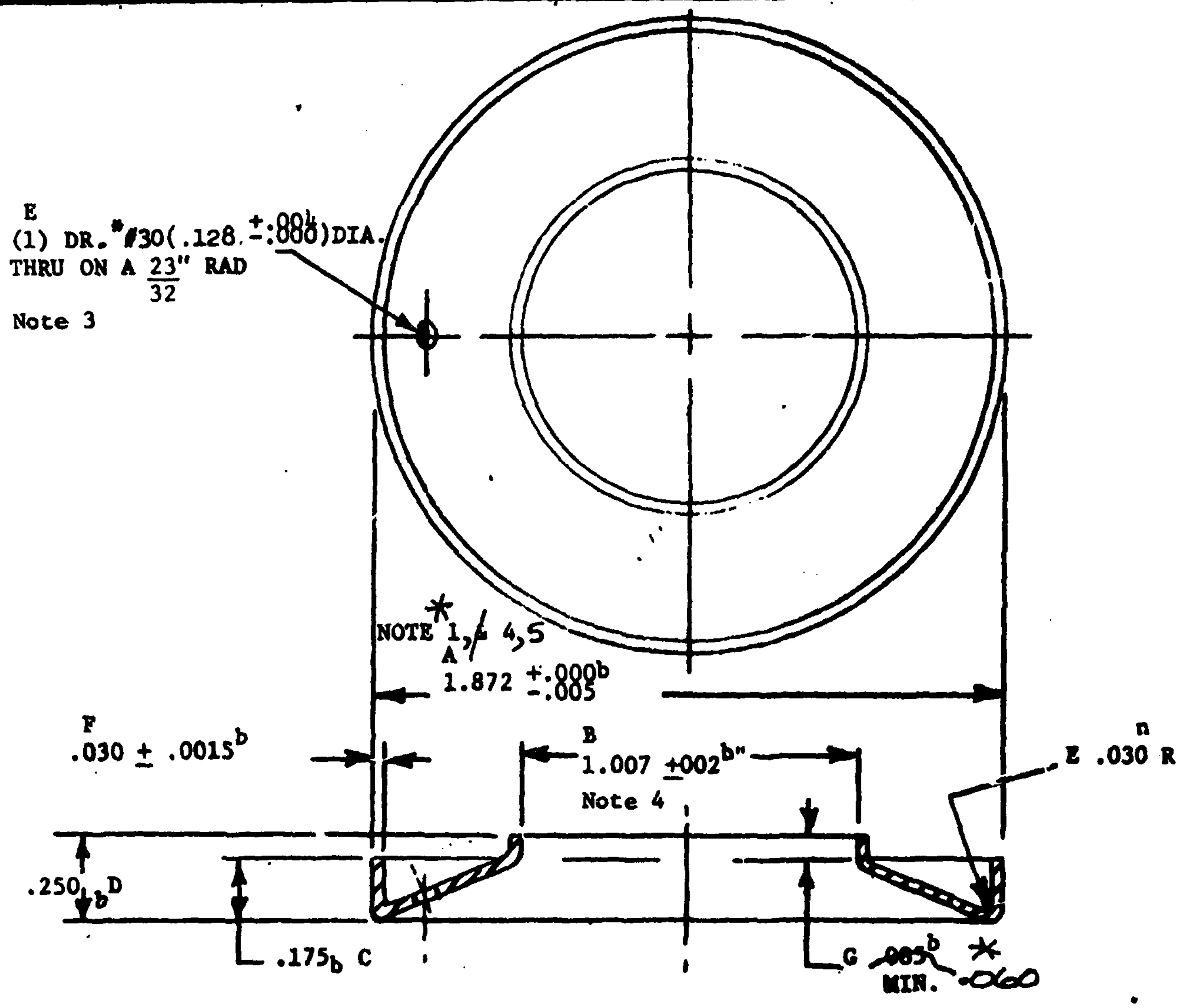
Product 3025260 ANODE WELD FLANGE

Date Sept. 14, 1977 Page 1.0

Engineering Specification 30-2-5260

Code 8-Eh

Super. ~~Aug. 24, 1977~~



①

NOTES:

1. NOT MORE THAN .002 TAPER PERMITTED ALONG O.D. OF PART b
2. PARTS MUST BE FREE OF BURRS; TOOL MARKS, & SCRATCHES b
3. .128 +.004 -.000 DIA. HOLE MAY BE PUNCHED n
4. DIA'S TO BE CONCENTRIC WITHIN .005 TIR b
* 5. DIAMETER TOLERANCE MAY VARY TO +.004 AT OPEN END OF DIAMETER.

MATERIAL: S10E2 TYPE 1010 (CRS)
.015 x 2.0 sq.

Basic Dimension	2 Place Dec.	3 Place Dec.
Up to 6"	± .02	± .005
Above 6" to 24"	± .03	± .010
Above 24"	± .06	± .015
Angular Dimension	± ½°	

FORMERLY LAB DRAWING A3025260R2

~~063-77-101-DLY/GAS~~

TL 308A

Engineering Standards will then make the engineering change to the specification and distribute the new printed materials to all using departments so that their standardizing bookkeeping will be updated.

E. Interface Control

A typical Engineering Change Notice (ECP) is shown in Figure 61, and official endorsers are shown in Figure 62. Although this change example is a rather simple one, it does show the mandatory approvers and the routing path required to make an engineering change (second sheet). The Specification, Figure 63, which is being changed is also included as an example.

F. Standardizing Procedure

The methods utilized in standardizing this product are described briefly below. Development and Production Engineering released information to the Engineering Standards Department via an Engineering Specification Request endorsed by authorized approvers from both Operations and Marketing. At this time, controlling Engineering Specifications were issued on the Transcalent rectifier. These specifications will be in effect throughout the Confirmatory and Pilot Run phases except as changed by an approved Engineering Change Notice. Initial and revised specifications are issued to the activities which require them, and it is the responsibility of the using activities to see that the latest specifications are available to the operators who fabricate the product. The using activity is also responsible for the up-to-date maintenance of its specification book or reference files.

The Engineering Specifications will contain the following mandatory requirements as a permanent, printed record:

1. Outline Drawing
2. Testing Specification
3. Bill of Materials
4. Parts and Assemblies Specification
5. Material Specifications
6. Process Specifications
7. Marking Specification
8. Packing Specification

This information will thus constitute the Product Base Line at the conclusion of the Pilot Run phase of the engineering contract. Government approval of any subsequent changes can be incorporated in any subsequent production contracts if required to assure the form, fit or function of the device.

G. Specification Availability

Initial and revised specifications are issued to the activities that require them, and it is the responsibility of the using activities to see that the latest specification available to the person or persons who use it with a minimum of delay. The using activity is responsible for the up-to-date maintenance of its specification books or files.

H. Standardized Examples

An example of a standardized part drawing is shown in Figure 64. The example is used to demonstrate the procedures utilized on all parts drawings. The material specification in the lower left-hand corner shows an RCA designation of sides which in turn delineates material composition and material tolerance in the RCA specification system.

Please note that each dimension has a clarifying capital letter, and each tolerance has a small letter. The capital letter identifies the dimension, whereas, the small letter denotes the inspection tool to be used to measure the dimension. See the example of small letter delineation in Figure 65.

A proprietary assembly procedure sheet is also standardized, but not included in this report. Notice that the assembly drawing, Figure 66, lists the parts by number and the top of the procedure sheet identifies the parts associated with the number via a parts list. The operations sheet spells out in detail each assembly step required to assemble the device. This feature will make it possible to establish Quality Control Audit Stations in the future, as required. The last example delineates the plating procedure as required to complete the fabrication of the assembly. The procedures described assure that the assemblies are put together by the same procedures at all times, a necessary factor of the MM&T program.

RCA Electro Optics and Devices

Engineering Standards | Lancaster, PA

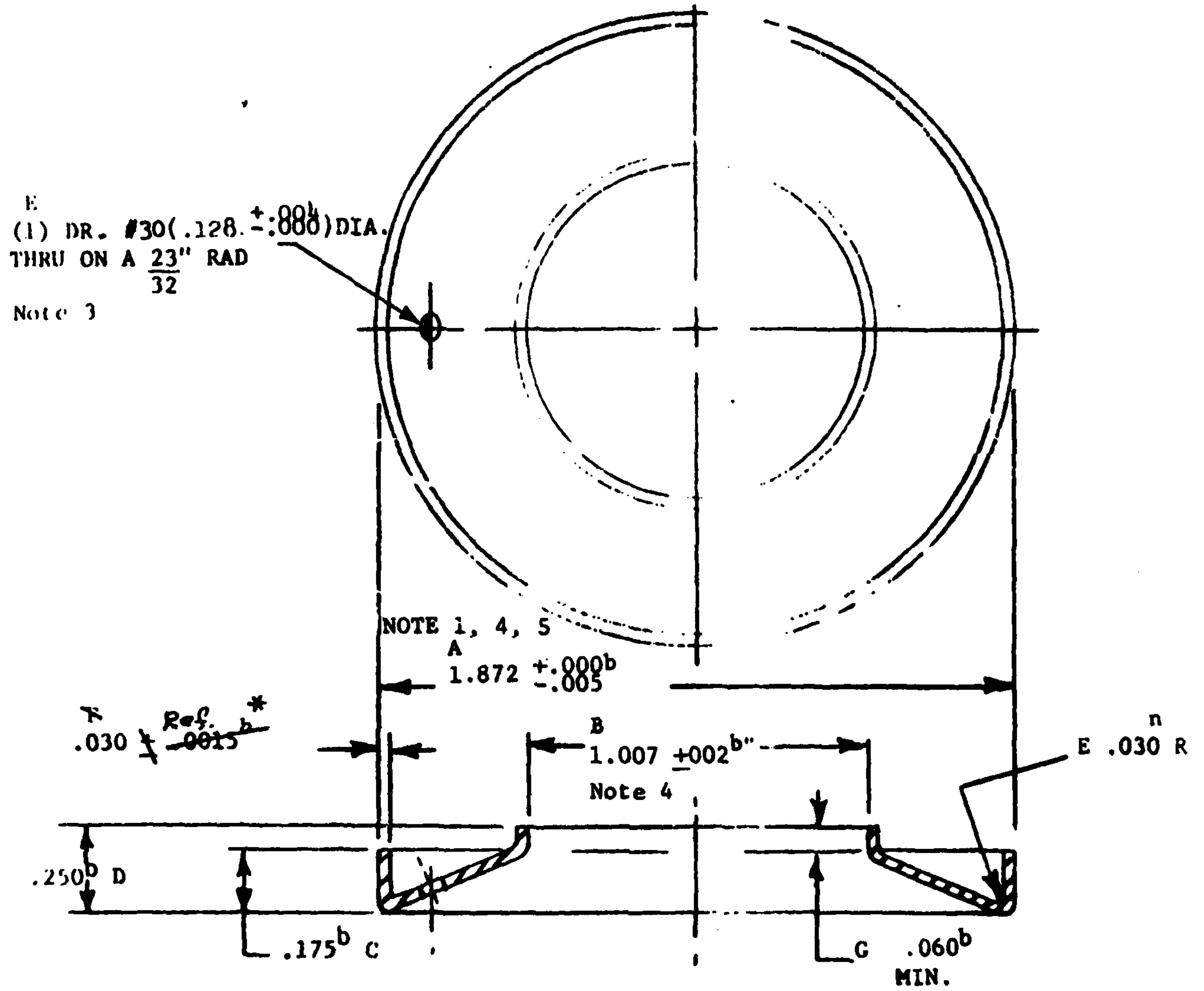
Subject 3025260 ANODE WELD FLANGE

Date ~~Mar. 23, 1978~~ July 19, 1978 Page 1.0

Engineering Specification 30-2-5260

Code 8-EH

Super. ~~Mar. 20, 1978~~ Mar. 23, 1978



①

NOTES:

1. NOT MORE THAN .002 TAPER PERMITTED ALONG O.D. OF PART[b]
2. PARTS MUST BE FREE OF BURRS; TOOL MARKS, & SCRATCHES[b]
3. .128 +.004 -.000 DIA. HOLE MAY BE PUNCHED[n]
4. DIA'S TO BE CONCENTRIC WITHIN .005 TIR[b]
5. Diameter tolerance may vary to +.004 at open end of diameter.

MATERIAL: S10E2 TYPE 1010 (CRS) * .030" ± F .0015 b X ~~.015 x 2.0 sq.~~ 2.0 sq.

Dimensions in inches.

Basic Dimension	2 Place Dec.	3 Place Dec.
up to 6"	± .02	± .005
Above 6" to 24"	± .03	± .010
Above 24"	± .05	± .015
Angular Dimension	± ½°	

FORMERLY LAB DRAWING A3025260R2 ~~963-78-108~~ ~~DLY/SDH~~ 963-78-114 DLY

TL 3096A

Fig. 65

RCA ElectroOptics and Devices

Engineering Standards|Lancaster, PA

Date Mar. 23, 1978 Page 3.0

Engineering Specification 30-2-5260

Subject 3025260-1 ANODE WELD FLANGE

Code 8-EH

Inspection Method

Super. Aug. 24, 1977

Dimension or Characteristics	Spec	Sampling Plan - AQL	Equipment Used	Remarks
A	P/PRINT	b = 1.5%	MICROMETER - O.D.	
B	P/PRINT	b	MICROMETER V-BLOCK & DIAL INDICATOR	
C	P/PRINT	b	MICROMETER	
D	P/PRINT	b	MICROMETER	
E	P/PRINT	n = one/lot		
F	P/PRINT	b	MICROMETER	
G	P/PRINT	b	MICROMETER	
NOTES				
1	P/PRINT	b	V-BLOCK & DIAL INDICATOR	
2	P/PRINT	b	FINGERNAIL	NONE BIG ENOUGH TO CATCH A FINGER-NAIL.
3.	P/PRINT	n = one/lot		
4.	P/PRINT	b	V-BLOCK & DIAL INDICATOR	

• CHANGE 963-78-108 DLY/SDH

RCA Electronic Components

Engineering Standards | Industrial Tube Division | Lancaster, PA.

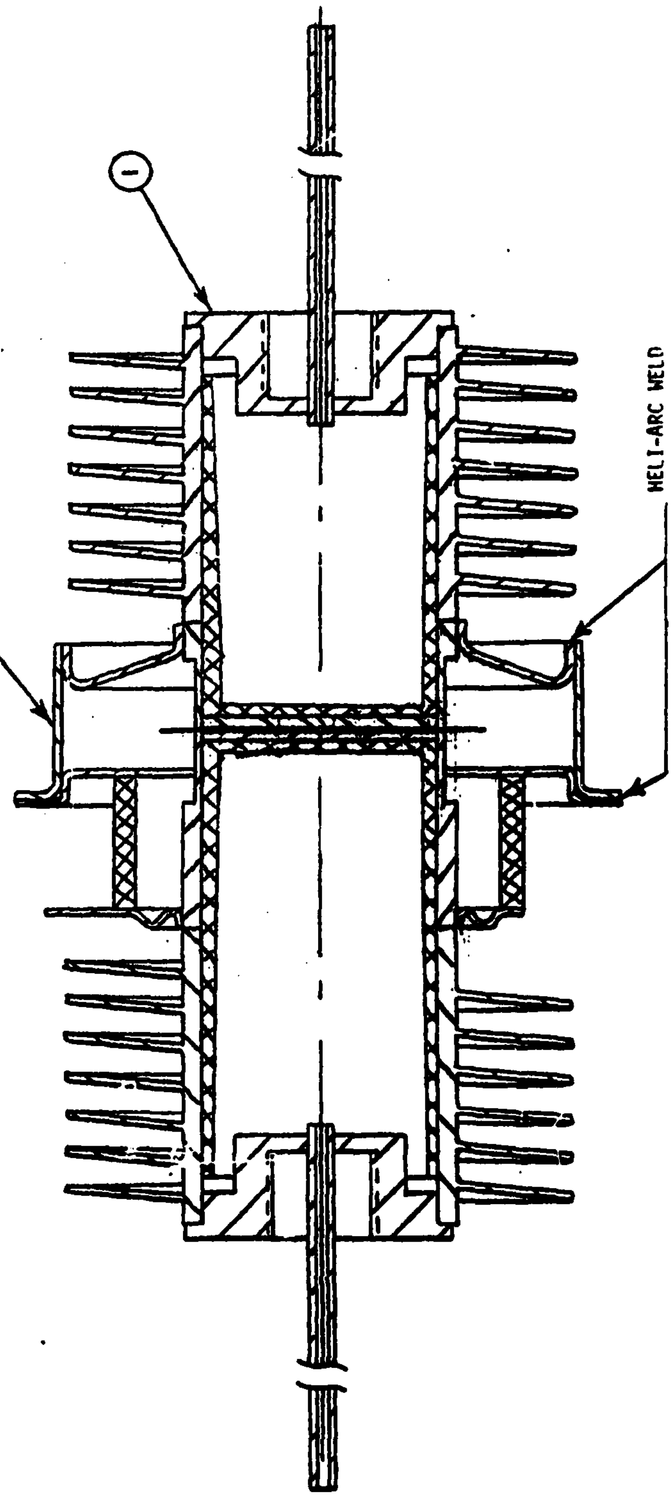
Subject RECTIFIER ASSLY, WELDED

Date June 9, 1980 Page 1.0

Engineering Specification 30-2-6367

Code 8-A

Super. Jan. 25, 1980, 3025294, Pg. 1.0



Formerly 3025617

SCALE

DIMENSIONS IN

CAUTION: Use only the lubricants specified in E.S. 33-73-005.
UNLESS OTHERWISE SHOWN. DIMENSIONS SHOWN WITHOUT TOLERANCES ARE DESIGN CENTERS

963-80-116 DLY/SDH

• CHANGE

I. Video Tape

All processes relative to manufacturing and testing were video taped. These video tapes were supplied to the government in accordance with the agreement made 3 April 1980 for the close out of this contract. In addition to the video tapes, a cross index for the Transcalent rectifier, thyristor and transistor was included.

VII. Program Evaluation and Review Technique

A Program Evaluation and Review Chart (PERT) was prepared quite early in the program. It contains the objectives for all the major portions of the contract along with the most critical path and delivery dates for all items. The chart was used as a management tool in the Transcalent Silicon Rectifier Program. The chart can be seen in Figure 67.

VIII. Conclusion and Recommendation

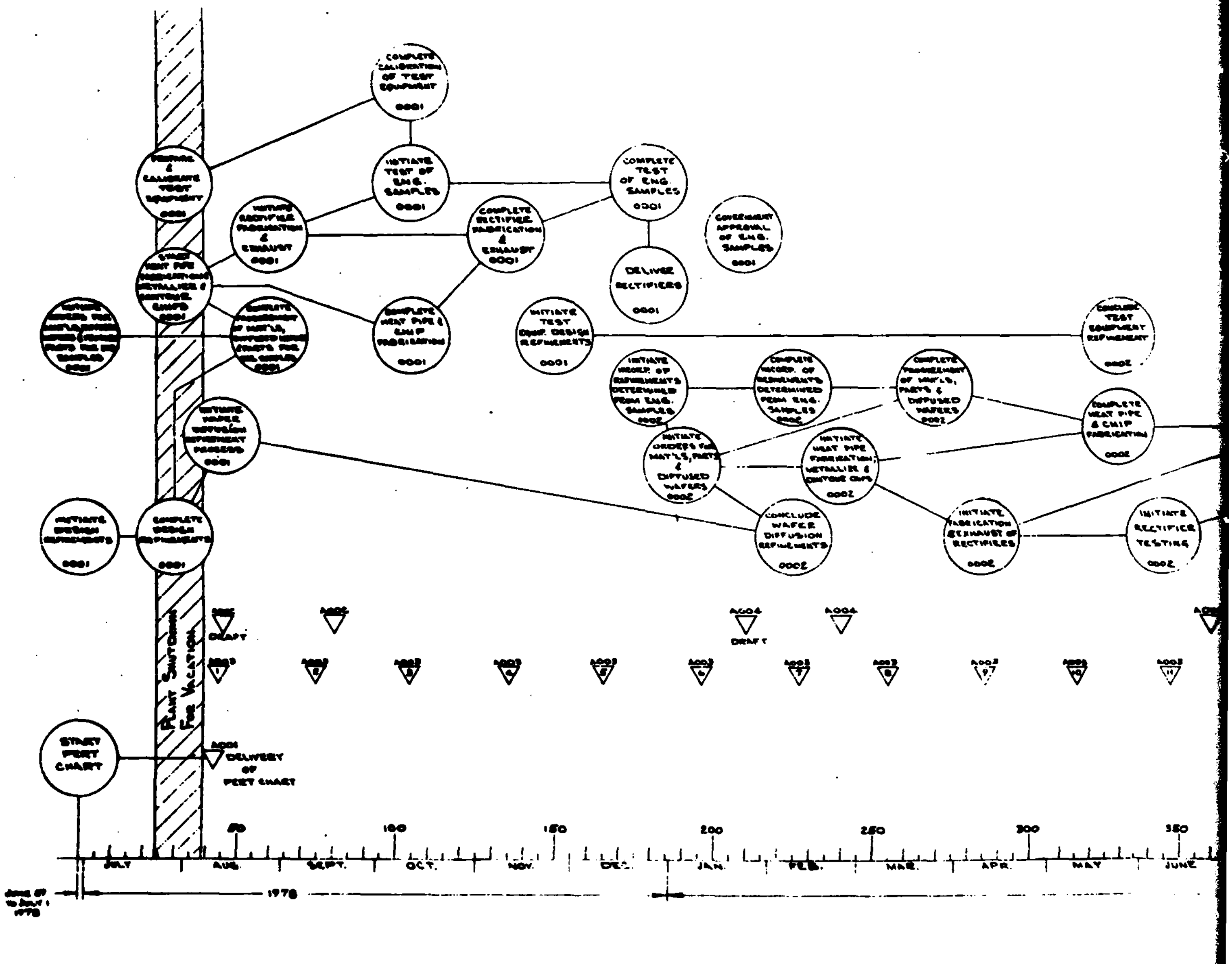
The engineering and confirmatory sample phases of the program were successfully completed on schedule as stipulated by the program evaluation chart (PERT).

No particular difficulties were involved in either phase of the program.

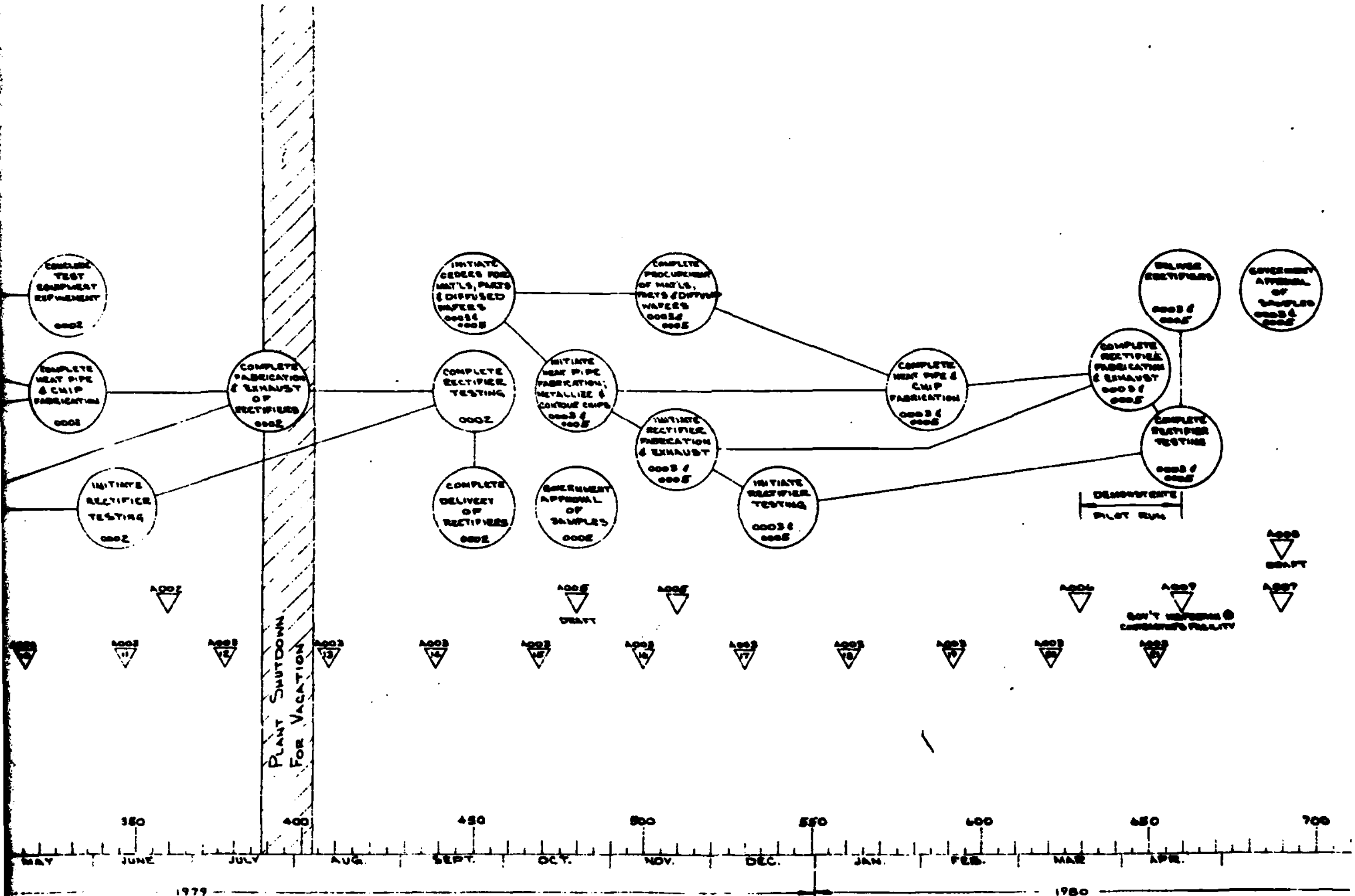
All drawings and procedures were updated to reflect the final design, namely, standard doped, webless wick and nonconvoluted cathode strain isolation rings. The reasons for the final design have already been discussed and verified in the body of this report. Copies of the detail assembly drawings were shipped to MERADCOM on 13 August 1980.

The Pilot run portion of the program is to be deleted as indicated in the RCA proposal No. DP-8135A for: "Manufacturing Methods and Technology for Silicon Rectifiers" dated 19 November 1979 and the agreement arrived at on 3 August 1980 at MERADCOM.

It is suggested that a contractor be found to continue with the Pilot run portion of the program.



COMPLETE CALIBRATION OF TEST EQUIPMENT 0001
INITIATE TEST OF ENG. SAMPLES 0001
COMPLETE TEST OF ENG. SAMPLES 0001
GOVERNMENT APPROVAL OF ENG. SAMPLES 0001
COMPLETE RECTIFIER FABRICATION & EXHAUST 0001
DELIVER RECTIFIERS 0001
COMPLETE HEAT PIPE & CHIP FABRICATION 0001
INITIATE TEST EQUIP. DESIGN REFINEMENTS 0001
CONCLUDE TEST EQUIPMENT REFINEMENT 0002
INITIATE WAFER DIFFUSION REFINEMENT PROCESS 0001
CONCLUDE WAFER DIFFUSION REFINEMENTS 0002
INITIATE FABRICATION EXHAUST OF RECTIFIERS 0002
COMPLETE HEAT PIPE & CHIP FABRICATION 0002
INITIATE RECTIFIER TESTING 0002
INITIATE DESIGN REFINEMENTS 0001
COMPLETE DESIGN REFINEMENTS 0001
PLANT SHUTDOWN FOR VACATION
DRAFT
DRAFT
START PERT CHART
A001 DELIVERY OF PERT CHART
50
100
150
200
250
300
350
JULY
AUG.
SEPT.
OCT.
NOV.
DEC.
JAN.
FEB.
MAR.
APR.
MAY
JUNE
1978



RCA PERT CHART
CONTRACT: DAAK 70-78-C-0120
PREPARED BY: B Adams June 30, 1978
DRAWN BY: R. McVey Aug. 7, 1978
APPROVED BY: R.E. Reed, Aug 9, 1978

Figure 67

IX. Distribution List

The following pages include the distribution list supplied by the Contracting Officer with the DD 1423 for the Interim Technical Report.

Dr. Paul E. Greene
Dir. Solid State Lab.
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Palo Alto, CA 94304

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Princeton, NJ 08540

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Murray Hill, NJ 07974

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Adelphi, MD 20783

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Fort Monmouth, NJ 07703

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Research Triangle Park, NC 27709

Naval Research Laboratory
ATTN: Dr. David F. Barbe,
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4555 Overlook Avenue, SW
Washington, DC 20375

Naval Electronics Lab Center
ATTN: Mr. Charles E. Holland, Jr.
Code 4300
271 Catalina Blvd.
San Diego, CA 92152

The Johns Hopkins Univ.
Applied Physics Laboratory
ATTN; Dr. Charles Feldman
11100 Johns Hopkins Road
Laurel, MD 20810

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Naval Surface Weapons Center
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Code WR-43
White Oak
Silver Spring, MD 20910

Commander
RADC
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Griffiss AFB, NY 13441

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Geo. C. Marshall Space Flight Center
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Marshall Space Flight Center, AL 35812

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Langley Research Center
Langley Station
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Hampton, VA 23665

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Fort George C. Meade, MD 20755

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OH 45433

Lincoln Laboratory, MIT
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P.O. Box 73
Lexington, MA 02173

RADC (ETSD)
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Hanscom AFB, MA 01731

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Semi-Conductor Products Dept.
Building 7, Box 42
Syracuse, NY 13201

Micro-Electronics Laboratory
Hughes Aircraft Company
500 Superior Avenue
Newport Beach, CA 92663

Silicon Transistor Corp.
ATTN: Mr. P. Fitzgerald
Katrina Road
Chelmsford, MA 01824

Mr. Daniel Becker
Reliability & Qual. Test Center
Mannes Spacecraft Center
Houston, TX 77058

Texas Instruments, Inc.
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P.O. Box 5012
Dallas, TX 75222

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168 Albion Street
Wakefield, MA 01880

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Westinghouse Electric Corp.
R&D Center
Pittsburgh, PA 15235

National Semi-Conductor Corp.
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Danbury, CT 06810

Solitron Devices
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Tappan, NY 10983

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Irvine, CA 92714

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Whippany, NJ 07981

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Power Systems Division
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South Windsor, CT 06074

Martin Marietta
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P.O. Box 179
Denver, CO 80201

J. J. Henry Co., Inc. Special Proj.
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Arlington, VA 22202

Fermi National Accelerator Lab.
ATTN: Mr. Frank S. Cilyo
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Washington, DC 20360

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Cambridge, MA 02139

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Harry Diamond Laboratories
ATTN: Technical Library
Connecticut Avenue and
Van Ness Street
Washington, DC 20438

Jet Propulsion Laboratory
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Goleta, CA 93017

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Houston, TX 77058

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Phoenix, AZ 85010

Lockheed California Co.
ATTN: Mr. W. W. Cloud
Department 75-82
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Plant A-1
Burbank, CA 91520

Sanders Associates
ATTN: Mr. A. Hurley
NCAI - 6247
95 Canal Street
Nashua, NH 03061

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ATTN: DDC-IRS
5010 Duke Street
Cameron Station (Bldg. 5)
Alexandria, VA 22314

NASA
Scientific & Tech. Inf. Off./KSI
Washington, DC 20541

Commander
U.S. Army Electronics Command
Communications Systems
Procurement Branch
Fort Monmouth, NJ 07703
ATTN: Capt. H. John Patch/PCO
DRSEL-PP-C-CS-1

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Defense & Space Systems Group
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Redondo Beach, CA 90278

Garrett Air Research
ATTN: Mr. Everett Geis
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Torrance, CA 90509

Airesearch Manufacturing Co.
ATTN: Mr. John Ashmore
Electronic Systems
2525 W. 190th Street
Torrance, CA 90509

Naval Underwater Systems Center
ATTN: Mr. George Anderson
Code 3642
Newport, RI 02840

Dr. Roy Scott Hickman
Chairman, Dept. of Mech & Environ.
Engr.
University of California
Santa Barbara, CA 93106

Ohio Semitonics, Inc.
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Columbus, Ohio 43212
ATTN: Mr. A. E. Middleton

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086-963

R. E. Reed (10)
086-963

J. Grosh/R. Bauder
080-923

C. E. Doner
086-963

G. J. Buchko/R. Beam
003-953

J. Heine
068-682

Library
686

R. M. Bowes
057-644

J. V. Platt
Somerville

K. C. Harding
Arlington

E. Schmitt
Somerville

B. B. Adams
086-963

J. D. Schmitt
057-634

M. F. DeVito
086-963

APPENDIX

RCA ACCEPTANCE TEST PROCEDURE (ATP)

SILICON TRANSCALENT RECTIFIER, J15401

CONTRACT:	DAAK70-78-C-0120 DATED: 78 Jun 30
ITEM NO.:	0004, DD1423 Seq. No. A002
PROJECT:	P331/E38/78
SPECIFICATION:	MERADCOM Semiconductor Device Silicon Transcalent Rectifier Spec dated 6 June 1978
PREPARED FOR:	U. S. Army Mobility Equipment R&D Command Procurement & Production Directorate Fort Belvoir, VA 22060
PREPARED BY:	RCA Corporation Solid State Division, Electro-Optics & Devices New Holland Avenue Lancaster, Pennsylvania 17604
ISSUE DATE:	May 30, 1979

FOREWORD

This test plan for the Confirmatory Samples, Item 0002, is submitted in fulfillment of the contract data requirement for a Product Assurance Test, Demonstration and Evaluation: Confirmatory Sample Test Plan, Item 0004, Seq. No. A002.

RCA forms TL-362, TL 343, and TL 309A are used for the Acceptance Specification list of tests and test methods. These forms are components of the RCA Configuration Management plan used for the control and direction of this contract.

This report is written also in conformance with paragraphs 1.2.6, 3.1.8, and 3.1.9 of Attachment No. 1 to the contract.

After receipt of this report, it is recognized that the government shall have 15 days in which to evaluate this test plan.

RCA Electronic Components

Lancaster, PA

TYPE J15401

Silicon Transcalent Rectifier

ACCEPTANCE SPECIFICATION

Date May 30, 1979

Supersedes Engineering Test Plan

Test Plan for Confirmatory Samples of Silicon Transcalent Rectifier, J15401

This Test Plan describes the tests and inspections to be performed on completed J15401 Transcalent Rectifiers.

Reference Specification: MERADCOM Semiconductor Device
Silicon Transcalent Rectifier Spec.
dated 6 June 1978

Test Plan

A. 1. Testing Time Schedule - After all assembly and manufacturing operations have been completed on finished J15401 units, these units are to be tested in accordance with this Test Plan.

2. Sequence of Examinations and Tests: Tests may be run in any order unless a specific order of tests is noted elsewhere. The listing of tests within any group or subgroup is not a specified order of tests.

3. Confirmatory Sample Inspection - The Confirmatory Sample Inspections shall consist of the tests specified in Tables I, II, and III. The number of confirmatory samples to be delivered to the Government is 10. The percentage of units to be subjected to each test and the percentage of failures allowed are listed below. When the percentage of units to be tested is less than 100%, the units shall be randomly selected. In all cases where a percentage selected for testing of failures allowed results in a fractional number of units, the quantity shall be rounded up to the next whole number of units.

Table I Group A Inspection

		% of Units to be Tested	% of Units Tested Allowed to Fail
Subgroup 1	Visual and Mechanical Inspection	100	0
	Physical Dimensions	100	0
Subgroup 2	Reverse Current and Reverse Voltage ($T_A = 25^oC$)	100	0
Subgroup 3	Thermal Resistance for Rectifier Diodes	100	10
Subgroup 4	Reverse Current and Reverse Voltage ($T_C = 125^oC$)	100	5

Table I Group B Inspection

		% of Units to be Tested	% of Units Tested Allowed to Fail
Subgroup 1	Forward Voltage	100	0
Subgroup 2	Surge Current	100	10
Subgroup 3	Reverse Recovery Time	100	10

Table III Group C Inspection

Subgroup 1	Barometric Pressure - Reduced	50	0
Subgroup 2	Blocking-Voltage Life Test	30	0
Subgroup 3	Thermal Shock	20	0
	Moisture Resistance	20	0
	Salt Atmosphere	20	0
Subgroup 4	Thermal Fatigue Test	100	10
Subgroup 5	Shock	20	0
	Vibration, Variable Freq.	20	0

METHOD OR PARA.	REQUIREMENT OR TEST	CONDITIONS	MIL STD 105 AQL. % DEF.	MIL STD 105 INSP. LEV. OR CODE	SYMBOL	LIMITS MIN.	LIMITS MAX.	UNIT
Test Plan (Continued)								
31.	Description of the method of Tests and Procedures:							
		TABLE I - GROUP A INSPECTION						
Ref.: MIL-STD-750B								
Subgroup 1								
2071	Visual and Mechanical Inspection							
2066	Physical Dimensions	(See Figure 1)						
Subgroup 2		$T_A = 25 \pm 3^{o}C$						
4016.2	Reverse Current and Reverse Voltage	A.C. Method, f - 60 Hz $V_r = 800$ V			i_r		15	mA
Subgroup 3		$T_A = 25 + 3^{o}C$						
Para. 34.	Thermal Resistance for Rectifier Diodes	Heating Conditions $I_{F1} = 250$ A Cooling Conditions: Airflow $\leq$150 CFM			$R_{\theta jc}$		0.2	$^{o}C/W$
Subgroup 4		$T_C = 125 \pm 6^{o}C$						
	Reverse Current	AC Method, F - 60 Hz			i_r		60	mA
4016.2	Reverse Voltage	$V_r = 800$ V						

METHOD OR PARA.	REQUIREMENT OR TEST	CONDITIONS	MIL STD 105 AQL % DEF.	MIL STD 105 INSP. LEV. OR CODE	SYMBOL	LIMITS MIN.	LIMITS MAX.	UNIT
	TABLE II - GROUP B INSPECTION							
Subgroup 1		$T_A = 25 \pm 3^oC$						
4011.3	Forward Voltage	I_F = 250 A (A.C. Avg.) Forced Air Cooled $\leq$150 CFM			V_F		2.0	V
Subgroup 2		$T_A = 25 \pm 3^oC$						
	Surge Current	I_f = 250 A (Avg.) A.C. f = 60 Hz One (1) Cycle Surge: 10 surges; one (1) per Min., Surge duration = 7 mSec (Min.) V_r = 800 V			i_f	4000		A
	FINAL MEASUREMENT							
	Subgroup 2	$T_A = 25 \pm 3^oC$						
4016.2	Reverse Current and Reverse Voltage	A.C. Method, f - 60 Hz V_r = 800 V			i_r		15	mA
Subgroup 3								
4031	Reverse Recovery Time	Use JEDEC Test circuit for T_{rr}, $I_{FM} \geq$ 50 A, 1/2 Sine Wave Pulse of 20 μSec max. base width (L = 1.3 μH and C = 10.0 μf)			t_{rr}		15.0	μSec

†: AS RECORDED
#: TO BE DETERMINED
* CHANGE
** ADDITION
*** DELETION

TL362 10/7'

METHOD OR PARA.	REQUIREMENT OR TEST	CONDITIONS	MIL STD 105 AQL. % DEF.	MIL STD 105 INSP. LEV. OR CODE	SYMBOL	LIMITS MIN.	LIMITS MAX.	UNIT
		TABLE III - GROUP C INSPECTION						
Subgroup 1								
1001.1	Barometric Pressure (Reduced)	$T_A = 25 \pm 3^oC$ $t = 1$ min. @ f = 60 Hz, 15 mm of Hg. pressure, Peak Value of $V_r = 800$ V						
Subgroup 2								
	Blocking Voltage Life Test	$T_c = 125 \pm 6^oC$						
Para B2.		t = 200 hr., Peak value of $V_r = 800$ V See Figure 2						
	FINAL MEASUREMENTS							
	Subgroup 2	$T_A = 25 \pm 3^oC$						
4016.2	Reverse Current and Reverse Voltage	A.C. Method, f - 60 Hz V_r = 800 V			i_r		15	mA
Subgroup 3								
1051.1	Thermal Shock (Temperature Cycling)	Test Condition B, 5 cycles except $T_{LOW} = -25^oC$						
1021.1	Moisture Resistance	Omit Initial Condition						
1041.1	Salt Atmosphere (Corrosion)	t = 24 hr.						
	FINAL MEASUREMENTS							
	Subgroup 3	$T_A = 25 \pm 3^oC$						
4016.2	Reverse Current and Reverse Voltage	A.C. Method, f - 60 Hz $V_r = 800$ V			i_r		15	mA

#: AS RECORDED
#: TO BE DETERMINED
* CHANGE
** ADDITION
*** DELETION

TL382 10/7

METHOD OR PARA.	REQUIREMENT OR TEST	CONDITIONS	MIL STD 105 AQL % DEF.	MIL STD 105 INSP. LEV. OR CODE	SYMBOL	LIMITS MIN.	LIMITS MAX.	UNIT
Subgroup 4								
Para. B3.	Thermal Fatigue Test	I_F = 250 A (Avg.) T_c = 30° + 10° min. T_c = 90° ∓ 10° max. Applied Voltage = 6 V min.				200		Cycles
	FINAL MEASUREMENTS							
	Subgroup 4	T_A = 25 ± 3°C						
4016.2	Reverse Current and Reverse Voltage	A.C. Method, f - 60 Hz V_r = 800 V			i_r		15	mA
Subgroup 5								
2016.2	Shock	Non-Operating, 500 G @ 1.0 mSec, 5 blows each in orientation: X_1, Y_1 and Z						
2056	Vibration, Variable Frequency	5 G, 100 Hz to 1000 Hz						
	FINAL MEASUREMENTS							
	Subgroup 5	T_A = 25 ± 3°C						
4016.2	Reverse Current and Reverse Voltage	A.C. Method, f - 60 Hz V_r = 800 V			i_r		15	mA
	Subgroup 3	T_A = 25 + 3°C						
Para. B4.	Thermal Resistance for Rectifier Diodes	Heating Conditions I_{F1} = 250 A Cooling Conditions: Airflow ≤150 CFM			$R_{\theta jc}$		0.2	°C/W

†: AS RECORDED
#: TO BE DETERMINED

- CHANGE
- ·· ADDITION
- ··· DELETION

TL382 10/77

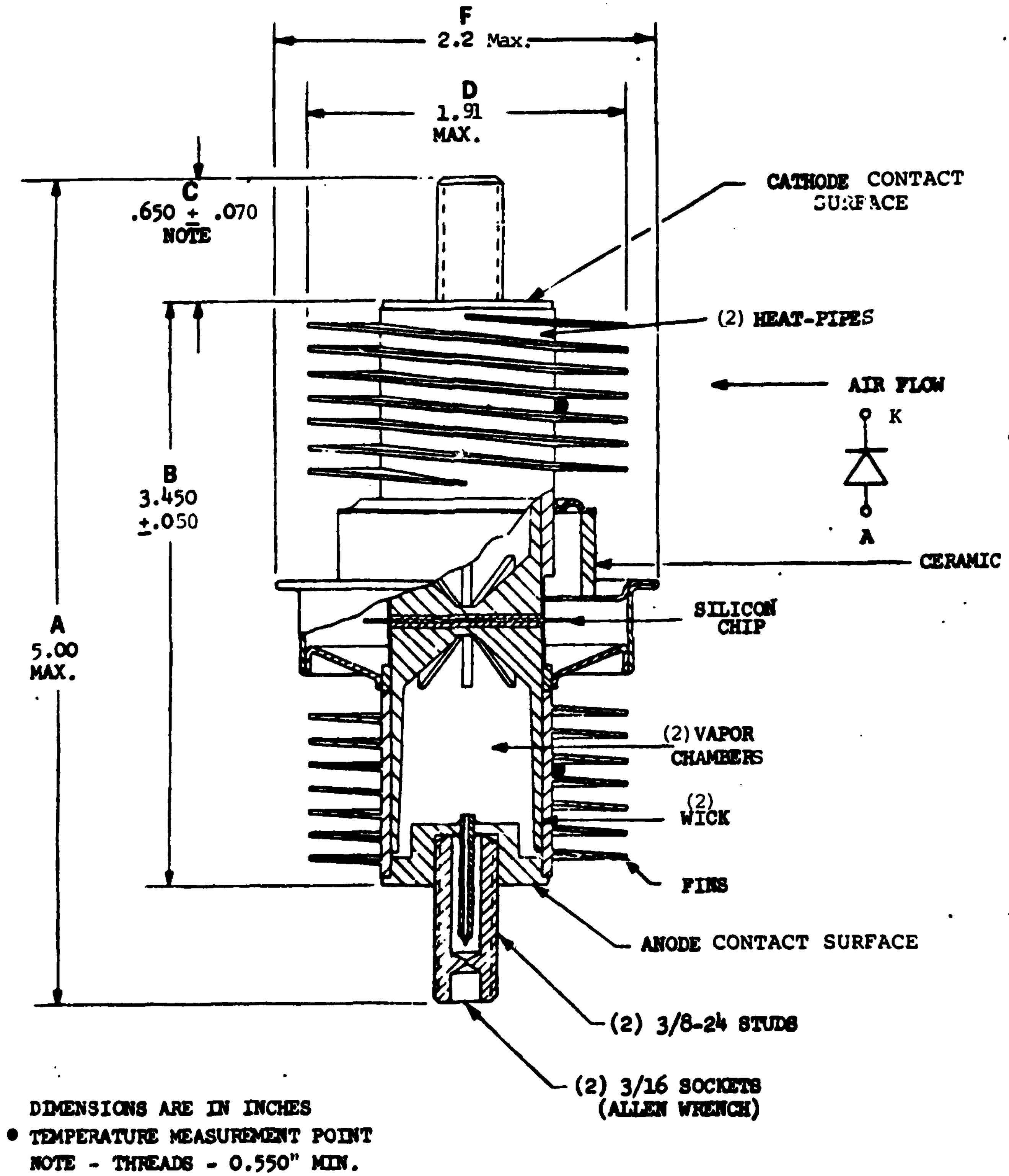

Figure 1 Transcalent Rectifier Type J15401 Cross Section

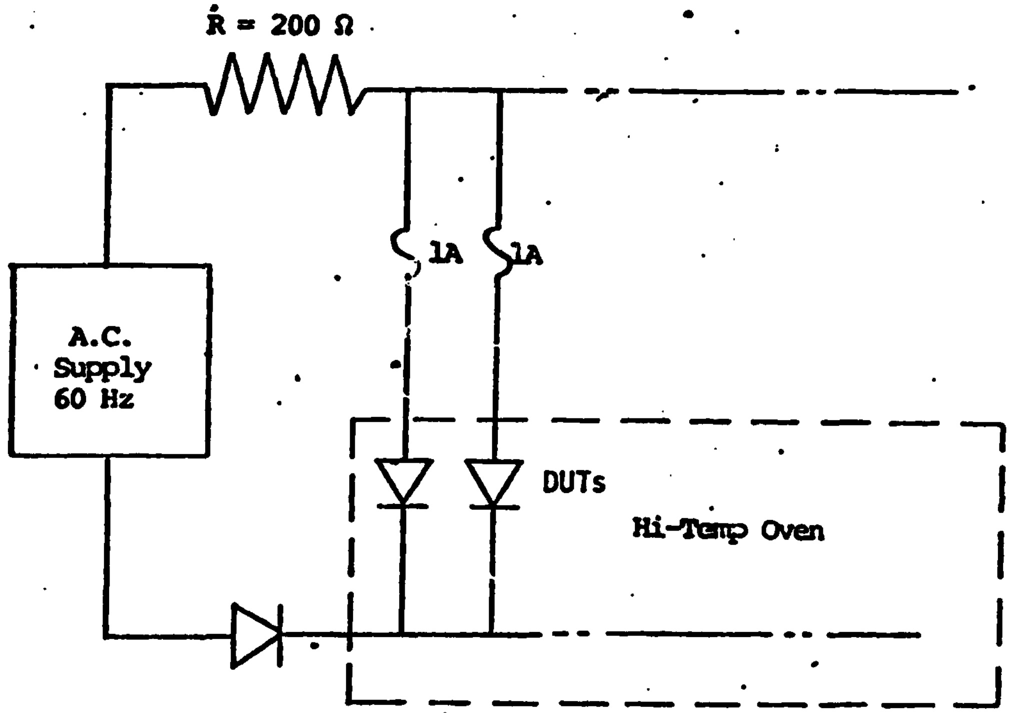

Figure 2 Basic Circuit for Blocking Voltage Life Test

B. 2. Blocking-Voltage Life Test

The sample to be tested shall be placed in the circuit of Figure 2. Test duration will be a minimum of 200 hours at a case temperature, $T_C = 125 \pm 6^{\circ}C$.

3. Thermal Fatigue Test - The device shall be cycle tested between two case temperatures $T_C = 30 \pm 10^{\circ}C$ and $T_C = 90 \pm 10^{\circ}C$ for 200 cycles. A cycle shall consist of two intervals: "On" for at least two minutes and "Off" for at least two minutes, as required to achieve the case temperature limits. The device being tested will be connected in a test fixture with sufficient air flow across the device to obtain the case temperature excursion of $30 \pm 10^{\circ}C$ to $90 \pm 10^{\circ}C$ within the cycle.

4. Thermal Resistance for Rectifier Diodes - The rectifier to be tested should be placed in a circuit described in MIL-STD-750B, Method 4081, Figure 1. The procedure of para. 3 applies but 3.1 shall be replaced by the following: The measurement of the case temperature T_C, is performed at the base of the fins on the heat-pipes after the device reaches thermal equilibrium. The junction temperature, T_j, is determined from the value of V_{F1} measured during the brief measurement interval and from the calibration curve of this temperature dependent variable. The thermal resistance, $R_{\theta jc}$, is calculated as follows:

$R_{\theta jc} = \frac{(T_j - T_C \text{ (Average)})}{Pd}$ ($^{\circ}$C/Watt) where: P is the product of the heating current and voltage, d is the duty factor of the heating current on-time to the total interval including the measurement interval.

Paragraph 4 of Method 4081 shall specify:

(a) Heating conditions

(b) Cooling conditions

5. Preparation for Delivery - Preparation for delivery shall be in accordance with MIL-S-195000E.

C. Inspection Equipment

Exhibit A of this Test Plan lists the Electrical and Environmental test equipment to be used for the inspections of Tables I, II and III.

EXHIBIT A

ELECTRICAL AND ENVIRONMENTAL TEST EQUIPMENT

Method	Test Description	Status of Facility	Date of Last Calibration
2066	Physical Dimensions	"Go-No-Go" Gauge Available	3/16/79
4016.2	Reverse Current	Facilities available for A.C. Method. Temperature Controlled Oven available. (Tek. Osc. Type 564 used for Parameter Measurement).	1/31/79
Par. B4	Thermal Resistance	Engineering Test Facility available.	4/27/79
4011.3	Forward Voltage	Power Supply and Monitoring available.	4/20/79
4066.2	Surge Current	Surge Fwd. Current and Rev. Voltage Supplies are available.	4/27/79
4031	Reverse Recovery Time	JEDEC Test Circuit developed and test results correlate with RCA, Somerville, NJ, test data. Test equipment is operational. (Tek. Osc. Type 564 used for Parameter Measurement).	1/31/79
1001.1	Barometric Pressure (reduced)	Vacuum Chamber and V_r Supply available. Supply modified for half-wave operation.	When used
Par. B2	Blocking-Voltage Life Test	Oven and Supply are available. Supply modified for half-wave operation. (Tek. Osc. Type 531A used for Parameter Measurement).	8/29/78
1051.1	Thermal Shock Temperature Cycling	Test facility available at RCA, Lancaster, Environmental Test Laboratory.	3/17/79 12/26/78
1021.1	Moisture Resistance	Ditto	12/15/78 3/17/79
2016.2	Shock	Ditto	When used
2056	Vibration, Variable Freq.	Ditto	4/11/79 5/2/79

EXHIBIT A (Cont.)

ELECTRICAL AND ENVIRONMENTAL TEST EQUIPMENT

Method	Test Description	Status of Facility	Date of Last Calibration
1041.1	Salt Atmosphere (corrosion)	Test facility available at RCA, Lancaster, Environmental Test Laboratory.	When used
Par. B3	Thermal Fatigue Test	Power Supply and Controller are available.	4/20/79

DRT 9/22/78
MFD 1/10/79
MFD 5/15/79